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# EDN

VOICE OF THE ENGINEER

Sept 15
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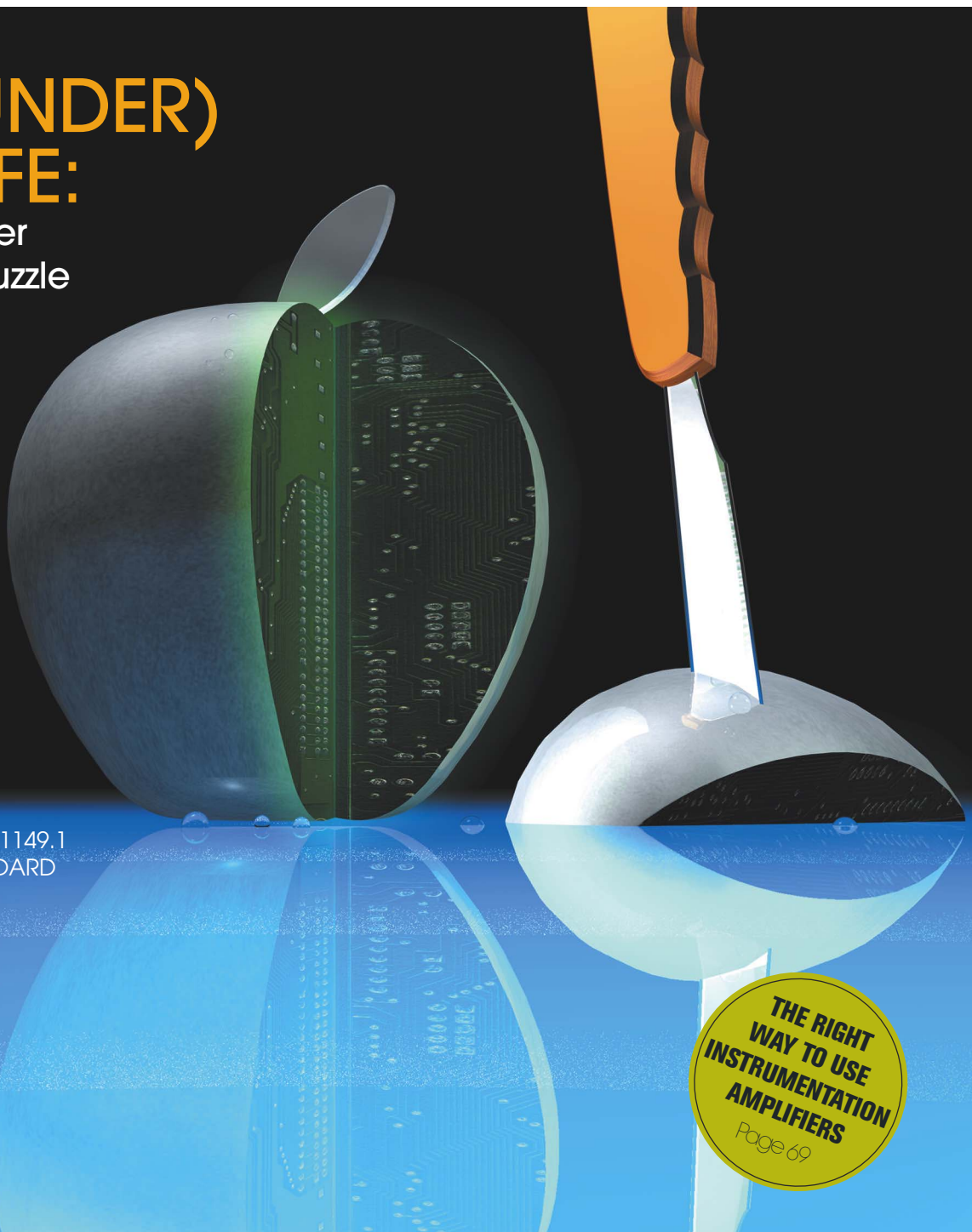

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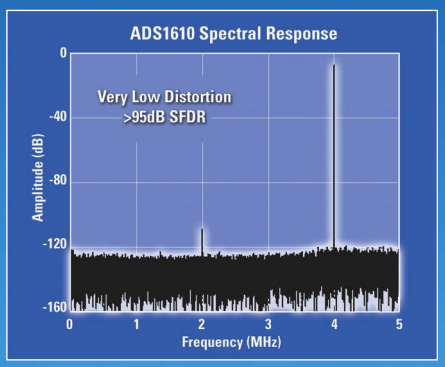


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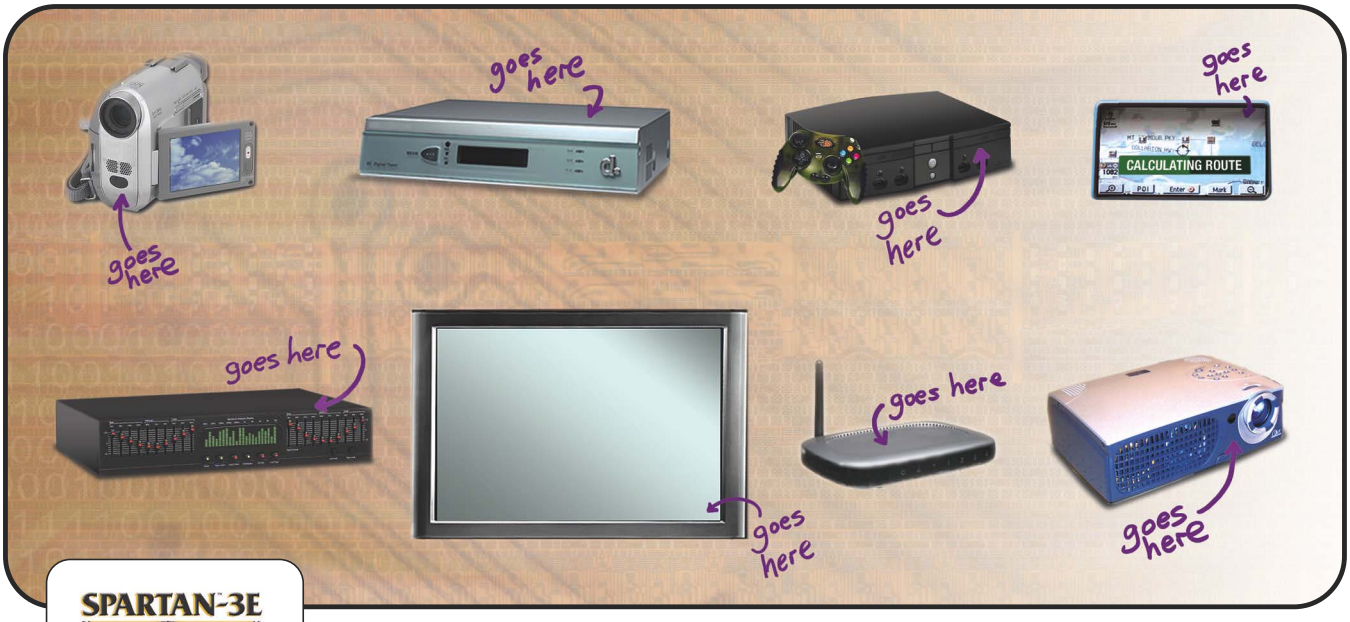


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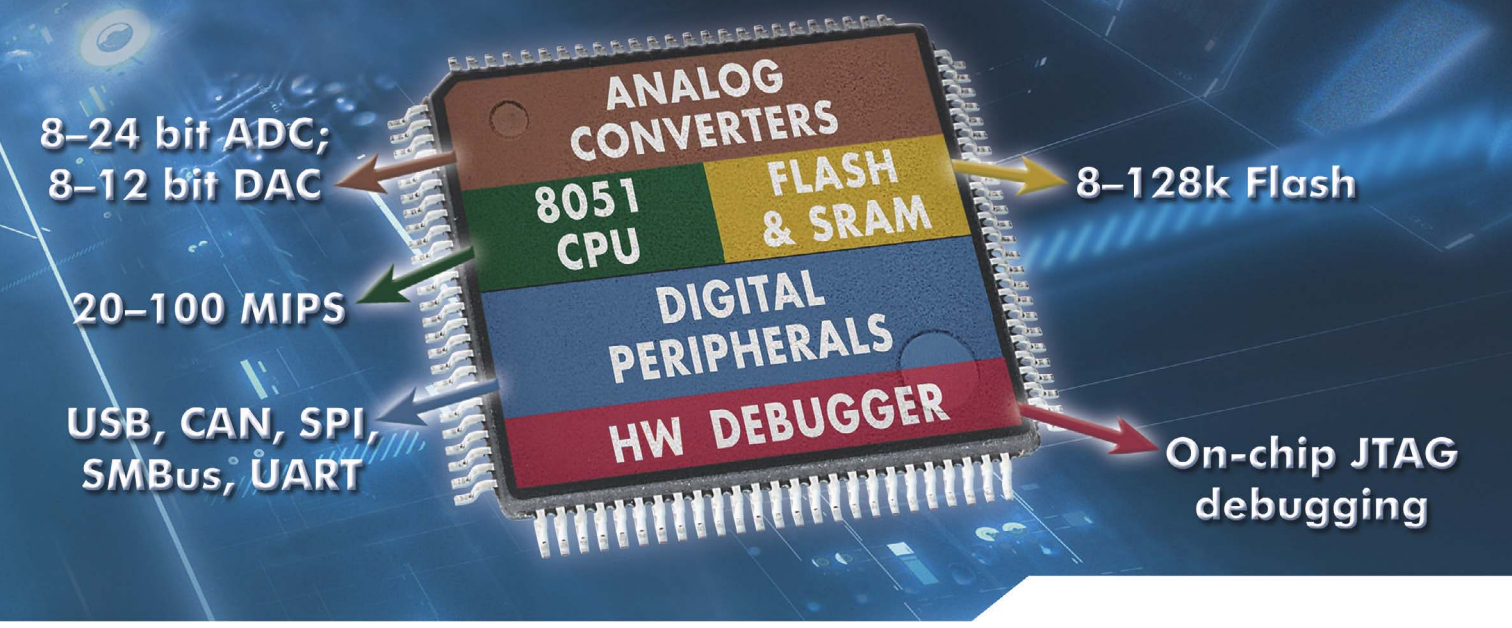


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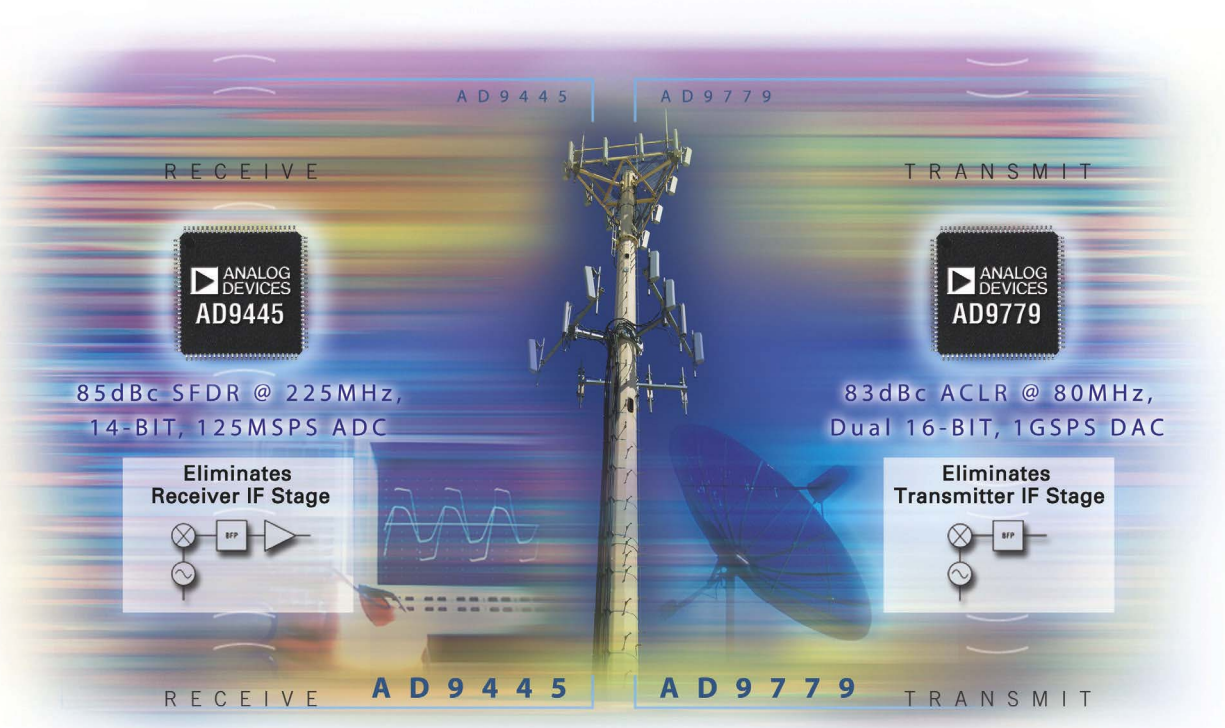


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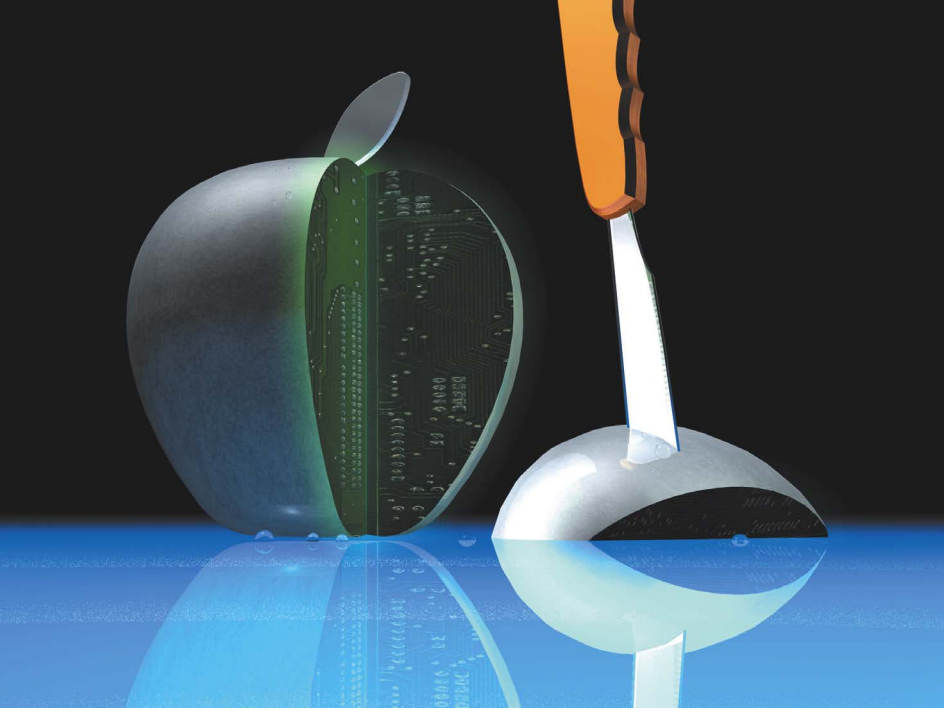

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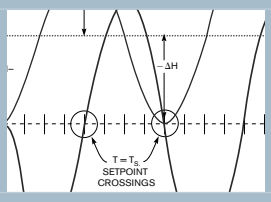

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## pulse






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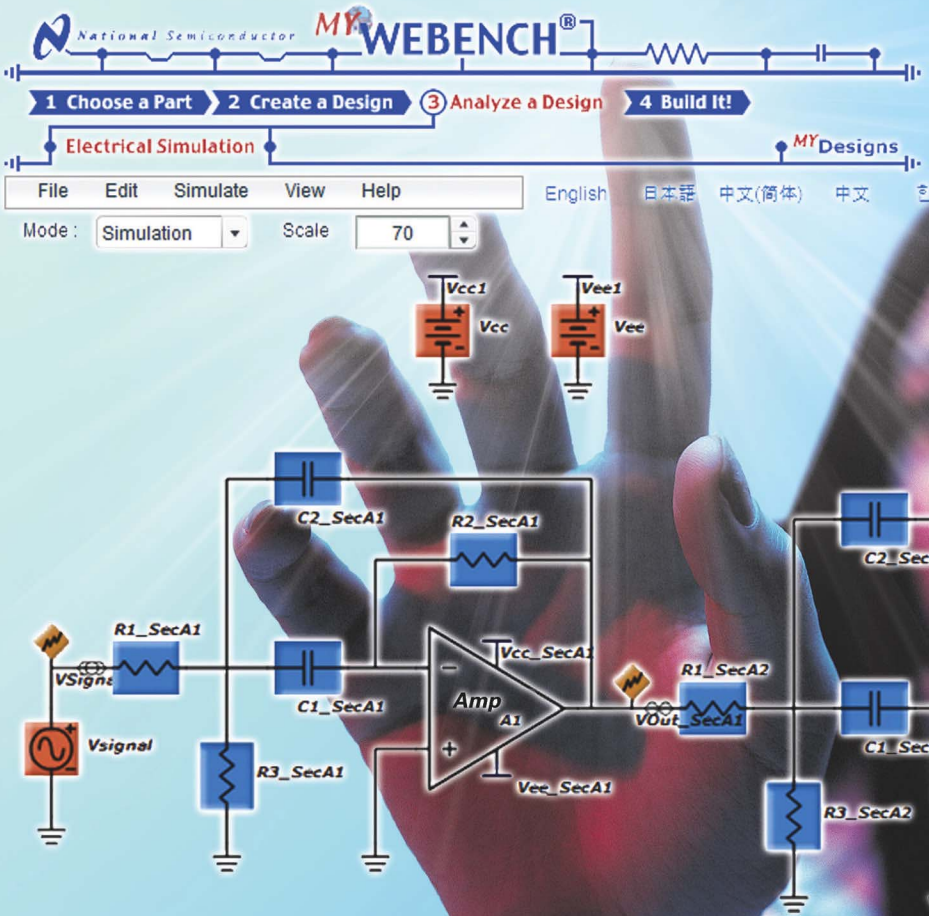


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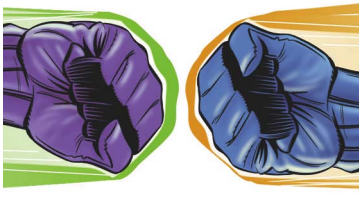

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BY BILL SCHWEBER, EXECUTIVE EDITOR

# Implementing standards: Think global, act local?

It's no secret that RFID is having trouble getting the tangible design-in success that it was supposed to achieve. Despite enormous effort and pressure from companies such as Wal-Mart, the practical challenges, costs, and unforeseen problems—especially when they combine hard-to-quantify benefits with excessively optimistic projections from pundits who should know better—are making large-scale RFID uptake a real struggle.

A recent article in *The Wall Street Journal* gave a different perspective on RFID possibilities (**Reference 1**). The article details how a 94-member cooperative of makers of Parmesan cheese in northern Italy successfully introduced RFID chips into their operation, which produces and handles several hundred thousand cheese wheels each year. Before you think this situation is trivial, look at the facts. The 30-kg (approximately 66-lb), tire-sized cheese wheels go through repeated aging cycles in climate-controlled warehouses for six to 36 months, and each wheel is repeatedly graded during the process, by color, tap-sounding timbre, and even X-rays. Cheese-wheel prices range from less than $200 for an average one to more than $350 for a top-grade one. Making Parmesan is not a casual hobby; despite first appearances, it is a serious business.

The cheese makers in the area agreed to try embedding RFID chips into the cheese crust, because the previous method of branding the crust had shortcomings. Among them, the branded number gradually faded as the cheese was handled, and the branding did nothing to prevent the serious problem of counterfeit cheese wheels entering the supply chain. With RFID, the cheese makers can uniquely track and update the status of each cheese wheel and assure buyers of the cheese's authenticity.

**The challenge for design engineers and their companies is to know their technologies and markets and decide how critical large-scale standards are to success.**

Admittedly, this application is specialized and unusual. But, in some ways, it represents a well-defined, tightly focused set of players with limited objectives. They are not trying to solve all of the problems of supply chains; they are just looking for an approach that works for them. The article states that the cooperative had invested less than $100,000 in the pilot program to test the system and about the same amount to fully implement it, plus 60 cents per RFID tag. With annual revenue of more than $380 million and RFID's reduction of tracking costs by about half, the cost-to-benefit ratio is favorable.

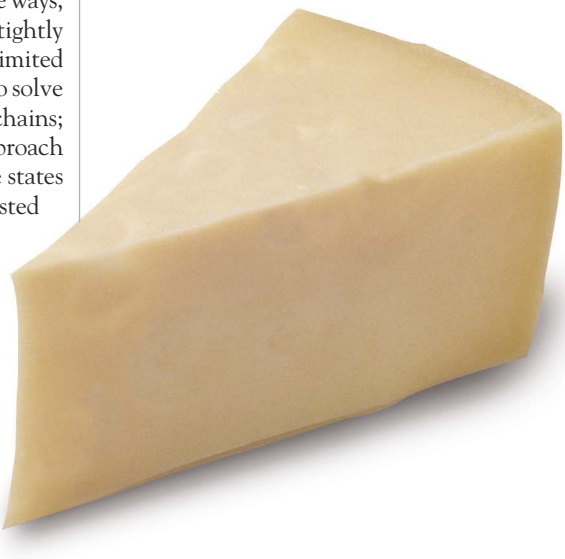
This application highlights the severely contradictory emotions our industry has about standards. On one side, they define a framework for functions and interoperability that some applications must have to succeed; a cell phone or DVD that doesn't meet a standard is useless. On the other side, standards can be excessively constraining or overwhelming; sometimes, they require substantial investment for completion of major infrastructure elements to succeed, all following those innumerable standards-committee meetings and votes.

The challenge for design engineers and their companies is to know their technologies and markets and decide how critical large-scale standards are to success. Is it better to use basic, available technology to solve a problem, albeit with an approach that may not have broader applicability? Or, should you wait for the broader standards to firm up? As usual, no one knows, and either way is a gamble. But matching the technical approach with the scope and timing of the problem is almost always a good idea. EDN

## REFERENCE

1 Kahn, Gabriel, "Who Made My Cheese? Tags Track Parmesan's Age, Origin," *The Wall Street Journal*, July 7, 2005, pg B1.

*Contact me at bschweber@edn.com.*



LEADING inside

A series of engineering insights
by Analog Devices.

# Specifying A/D Converters: Considerations for IF-Sampling Applications

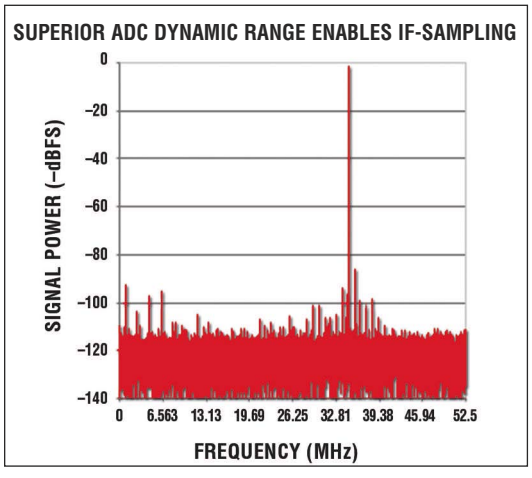
Choosing the ADC with the highest resolution or sampling speed is often not enough to satisfy the performance demands presented by IF-sampling architectures. ADCs for IF-sampling applications must support high input frequencies while also maintaining adequate SNR, SFDR, and SINAD performance. These features enable designers to eliminate one or more mixing stages and simplify filtering, thereby reducing cost and helping to meet end-system objectives.

Wideband signals having complex modulation—such as those used in many wireless communications, instrumentation, and radar systems—can exhibit time-varying bursts and transients. Furthermore, the data carried by these signals is often spread over multiple channels.

The ADC for these types of architectures must have sufficient input bandwidth to adequately capture and digitize this data. The ADC's dynamic range must also be high enough to detect small signals in the presence of blockers or other large signals in the bandwidth of interest.

### Dynamic Range and Noise Requirements

In wideband CDMA systems having a base data rate of 3.84 MHz, data converter clock rates of 16×, 20×, 24×, and 32× are viable. A data converter running at 92.16 MSPS provides good noise performance, and 16-bit ADCs that sample at 100 MSPS are available today. If lower sampling rates are used, the SNR required increases by 1 dB for 76.8 MSPS and 2 dB for 61.44 MSPS.




*32k point single-tone FFT/ADC: 105 MSPS, 70.3 MHz $A_{IN}$*

The receiver conversion gain and noise figure (NF) sets the ADC's required SNR. At the antenna, the noise spectral density is –174 dBm/Hz, or that of thermal noise. For a conversion gain of 40 dB and a noise figure of 3 dB, the noise spectral density (NSD) at the ADC input will be –131 dBm/Hz (–174 + 40 + 3). If the ADC noise floor is 10 dB below that of the front end noise, it will contribute about 0.1 dB to the overall NF of the receiver. Therefore, a maximum ADC noise floor of –141 dBm/Hz is desirable.

For IF-sampling applications, the total noise of the ADC can be determined by simple integration. For example, a 10 MHz bandwidth signal would have total noise of –71 dBm. This is calculated by adding the effect of the 10 MHz bandwidth [10 log (10 MHz) = 70 dB] to the 1 Hz noise floor of –141 dBm. If the full scale range of the ADC is 4 dBm, the required minimum full-scale SNR for the ADC is then 75 dB.

### Selecting the Optimum A/D Converter

What types of ADCs meet the needs of IF-sampling architectures? Typically, they require ADCs with 14 bits to 16 bits of resolution that deliver superior SNR at high input frequencies. Advances in high speed ADC technology offer improved SNR, low additive jitter, higher sampling rates, and increased input frequency capability. These features enable engineers to design more efficient base stations, radar, and measurement equipment.

Additionally, the instrumentation used to validate communications systems must meet even tighter specifications, so as not to mask or distort the end-product's actual performance. These systems allow designers to accurately characterize signals of interest with minimum added distortion from the data converter. The AD9446 16-bit, 100 MSPS ADC from Analog Devices is an example of wideband converter technology that is targeted for IF-sampling applications in communications instrumentation. With a 70 MHz analog input and 100 MSPS sampling rate, the AD9446 provides a spurious-free dynamic range of 83 dB; it provides 82 dB of SFDR with a 100 MHz analog input. For more information on the AD9446 and other data converters for IF-sampling applications, please visit *www.analog.com/PerformanceADCs.*

*Author Profile: **Joanne Mistler** is a marketing engineer with Analog Devices' High Speed Converter Group in Wilmington, MA. She has 22 years of RF/MW experience, focusing on low noise synthesizer design, digital communications, and test and measurement applications.*

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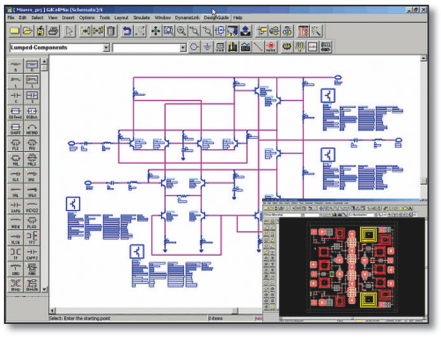

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| | Flash | RAM | # of Timers | Ch. | UART | I²C | SPI | CAN | # of ch. | # of ch. | Pins | (Ext.) | (Mhz) | | |
| LPC2104 | 128K | 16K | 4* | 6 | 2 | 1 | 1 | – | – | – | 32 | 16(3)/16 | 60 | 0° to +70° | LQFP48 |
| LPC2105 | 128k | 32K | 4* | 6 | 2 | 1 | 1 | – | – | – | 32 | 16(3)/16 | 60 | 0° to +70° | LQFP48 |
| LPC2106 | 128K | 64K | 4* | 6 | 2 | 1 | 1 | – | – | – | 32 | 16(3)/16 | 60 | 0° to +70° -40° to +85° | LQFP48 |
| LPC2114 | 128K | 16K | 4* | 6 | 2 | 1 | 2 | – | 4/10 | – | 46 | 19(4)/16 | 60 | -40° to +85° | LQFP64 HVQFN64 |
| LPC2119 | 128K | 16K | 4* | 6 | 2 | 1 | 2 | 2 | 4/10 | – | 46 | 19(4)/16 | 60 | -40° to +85° | HVQFN64 LQFP64 |
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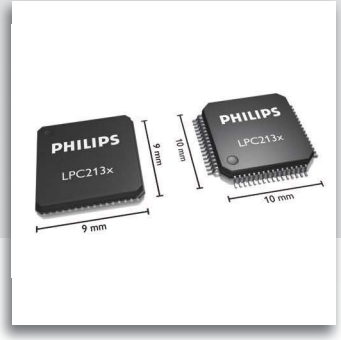
| LPC2131 | 32K | 8K | 4* | 6 | 2 | 2 | 2 | – | 0 | 0 | 47 | 22(4)/16 | 60 | -40° to +85° | LQFP64 |
| LPC2132 | 64K | 16K | 4* | 6 | 2 | 2 | 2 | – | 1 | 1 | 47 | 22(4)/16 | 60 | -40° to +85° | HVQFN64 LQFP64 |
| LPC2134 | 128K | 16K | 4* | 6 | 2 | 2 | 2 | – | 2/8 | 1 | 47 | 22(4)/16 | 60 | -40° to +85° | LQFP64 |
| LPC2136 | 256K | 32K | 4* | 6 | 2 | 2 | 2 | – | 2/8 | 1 | 47 | 22(4)/16 | 60 | -40° to +85° | LQFP64 |
| LPC2138 | 512K | 32K | 4* | 6 | 2 | 2 | 2 | – | 2/8 | 1 | 47 | 22(4)/16 | 60 | -40° to +85° | HVQFN64 LQFP64 |
| LPC2194 | 256K | 16K | 4* | 6 | 2 | 1 | 2 | 4 | 4/10 | – | 46 | 19(4)/16 | 60 | -40° to +85° -40° to +125° | LQFP64 |
| LPC2210 | Ext. | 16K | 4* | 6 | 2 | 1 | 2 | – | 8/10 | – | 76 | 19(4)/16 | 60 | -40° to +85° | LQFP144 |
| LPC2212 | 128K | 16K | 4* | 6 | 2 | 1 | 2 | – | 8/10 | – | 112 | 19(4)/16 | 60 | -40° to +85° | LQFP144 |
| LPC2214 | 256K | 16K | 4* | 6 | 2 | 1 | 2 | – | 8/10 | – | 112 | 19(4)/16 | 60 | -40° to +85° | LQFP144 |
| LPC2290 | Ext. | 16K | 4* | 6 | 2 | 1 | 2 | 2 | 8/10 | – | 76 | 19(4)/16 | 60 | -40° to +85° | LQFP144 |
| LPC2292 | 256K | 16K | 4* | 6 | 2 | 1 | 2 | 2 | 8/10 | – | 112 | 19(4)/16 | 60 | -40° to +85° | LQFP144 |
| LPC2294 | 256K | 16K | 4* | 6 | 2 | 1 | 2 | 4 | 8/10 | – | 112 | 19(4)/16 | 60 | -40° to +85° -40° to +125° | LQFP144 |

*Includes Watchdog Timer and Real-Time Clock

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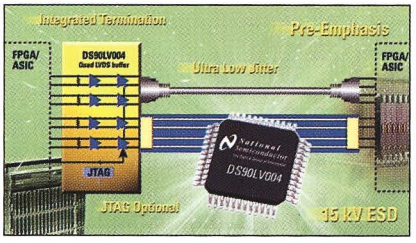
Vol. III, Issue 9

ANALOG edge℠

DESIGN idea: Enabling HDTV Capabilities ▶▶▶

# Featured Products

## World's First Four-Channel LVDS Buffer with Configurable Pre-emphasis




The DS90LV004 extends cable and backplane driving distances, boosts weak FPGA and ASIC LVDS signals, improves signal quality over lossy interconnects, and has 15 kV ESD protection from off board ESD strikes.

This device is a four channel LVDS buffer and repeater that operates up to 1.5 Gbps over the entire supply voltage and temperature operating range. High-speed data paths and flow-through pin out minimize internal device jitter and simplify board layout. In addition, the configurable pre-emphasis feature overcomes ISI jitter effects from lossy backplanes and cables.

The differential inputs accept LVDS and Bus LVDS signals such as those on National's 10-, 16-, and 18- bit Bus LVDS SerDes, as well as CML and LVPECL. The differential inputs are internally terminated with a 100Ω resistor to improve performance and minimize board space. The repeater function is especially useful for boosting signals for longer distance transmission over lossy cables and backplanes.

### Features

- 1.5 Gbps data rate per channel
- Configurable pre-emphasis drives lossy backplanes and cables
- LVDS/CML/LVPECL compatible input, LVDS output
- On-chip 100Ω input termination
- 15 kV ESD protection
- Single 3.3V supply
- Industrial -40 to +85°C temperature range
- See SCAN90004 for JTAG-enabled version

The DS90LV004 is ideal for buffering LVDS signals in office imaging systems, video systems, medical imaging, telecom, datacom, industrial, and automotive applications. The DS90LV004 is available in TQFP-48 packaging.

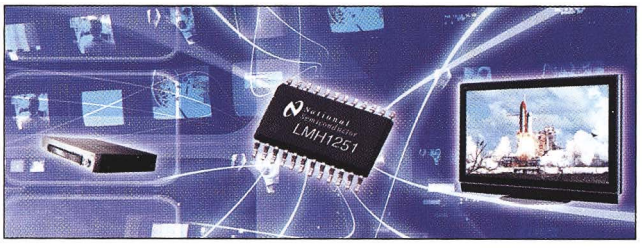
**www.national.com/pf/DS/DS90LV004.html**

## Industry's First High-Definition Video ($YP_BP_R$) to RGBHV (VGA) Video Decoder IC

The LMH1251 is a $YP_BP_R$ to RGBHV decoder with an integrated wideband 2:1 analog video switch. The device accepts one set of $YP_BP_R$ inputs and one set of RGB/HSync/VSync inputs. Based on the input selected, the output will be either a decoded TV or buffered PC video signal. The LMH1251 is capable of driving and/or processing 480i, 480p, 1080i, 1080p, XGA, SXGA, and UXGA video formats, which makes it an ideal solution for enhancing value in applications ranging from LCD monitors and set-top boxes to professional video equipment. Format conversion is done in the analog domain to preserve signal integrity and maintain picture clarity.

### Features

- $YP_BP_R$ to RGBHV conversion within 1% accuracy
- $YP_BP_R$ path: 70 MHz -3 dB Bandwidth
- RGB path: 400 MHz -3 dB Bandwidth
- Supports PC video display resolutions up to UXGA (1600 x 1200 @ 75 Hz)
- Sync separator and processor
- Smart video format detection for 480i, 480p, 720p, 1080i, and 1080p
- Power save mode
- Integrated 2:1 mux




The LMH1251 is ideal for use in TFT LCD monitors, set-top boxes, and projectors, video format conversion systems, video editing and broadcast equipment. The LMH1251 is available in a TSSOP-24 package.

**www.national.com/pf/LM/LMH1251.html**

# DESIGN | *idea*

*Cliff Win, Jr., Applications Engineer*
National Semiconductor

## Enabling HDTV Capabilities in Today's Systems

High Definition TV (HDTV) is now more prolific than ever. With a tremendously distinguishable difference in picture quality from traditional NTSC video, there is good reason why HDTV has been receiving high acclaim from videophiles as well as lay consumers. Today, the adoption of HDTV by the broadcast industry is on the incline as the percentage of worldwide TV service operators rapidly increases the offering of HD programming. Even video game console makers have joined the High Definition Video movement in recent years.

Now, taking a closer look at HDTV in terms of scanning format and active video lines per frame, "720p" and "1080i" are both designated as HD. 720p has 720 active lines per frame which are scanned progressively and 1080i has 1080 active lines per frame which are scanned in the interlaced mode. Another format, called Enhanced Definition (EDTV) or SDTV, is an alternative to HD. EDTV is not true High Definition per se, but an alternative video format under the 480p standard. EDTV is quite arguably the next best thing to HDTV and offers the standard 480 active video lines; however, the scanning format is progressive. This makes for a significant step forward in image quality.

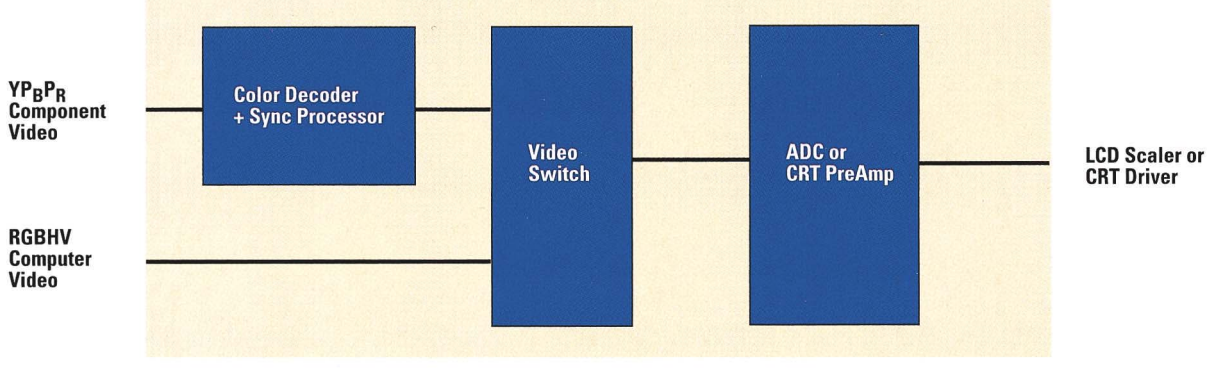
In order to utilize the advantages of EDTV and HDTV, a few things are necessary:

- Video transmission via the $YP_BP_R$ component standard: composite video cabling is only appropriate for NTSC video, and although S-video may be sufficiently acceptable for EDTV, HDTV should strictly use $YP_BP_R$ components.
- A video source that is capable of outputting such signals: for example, only a Progressive Scan DVD player is able to provide video in the 480p format, which in fact is the native resolution of DVDs.
- A television or display monitor that is capable of handling such signals as inputs: most of the standard analog TVs do not have the line rate capability to display any format beyond 480 Interlaced. A progressive scan TV set such as an EDTV or HDTV is thus required.

Due to these requirements, EDTV and HDTV sets are clearly more expensive than the common interlaced TV. However, if the timing capabilities of the display monitor are the impediment, there is an alternative for viewers to still enjoy progressive scan or HD video content. Computer graphics displays such as LCD and CRT monitors are certainly capable of handling the timing requirements of such signals. PC monitors are essentially HD display sets, though there is one caveat – they employ the RGBHV video standard rather than the $YP_BP_R$ video standard.

In the $YP_BP_R$ color space, color information is determined by two separate chrominance signals ($P_B$ and $P_R$), which are also a function of a third signal, the luminance signal. Horizontal and Vertical Sync are then compositely embedded onto this luminance signal. In the computer graphics video color space, color is defined by primary Red, Green, and Blue components, and Horizontal and Vertical Syncs are separated into two individual signals. The components of the $YP_BP_R$ and RGB color spaces are related by a matrix algebraic relationship, with the

**Figure 1: System Block Diagram**



coefficients of the matrices varying from format to format, i.e. SDTV, HDTV, etc. Thus, the components of the $YP_BP_R$ can be decoded into RGB accordingly. Such processing along with sync separation will effectively provide a complete $YP_BP_R$ to RGBHV conversion which enables progressive scan DVDs, HD video, or video game consoles to directly drive PC display monitors.

Although there are quite a few ways to convert $YP_BP_R$ to RGBHV, key considerations for implementation are cost, color space decoding precision, sync processing performance, and minimal impact to system architecture. The two solutions on the market today are a discrete design or integration into a very high-priced digital video processor. Both of these solutions compromise color decoding quality and system cost effectiveness. Carrying out the conversion discretely is cumbersome, requiring a number of devices and board space. Depending on the desired color accuracy, the discrete design can pose an additional challenge for design engineers. On the other hand, highly integrated digital video processors that may include the $YP_BP_R$ to RGBHV conversion are bundled with an excess of functions and features which makes them very cost inefficient. Ideally, a single monolithic IC that would increase quality and reduce cost over these existing $YP_BP_R$ to RGBHV solutions is desired. Further, this single-chip solution should be a direct drop into the signal path, easing system design and accelerating time-to-market. A simple block diagram of a possible system architecture is shown in ***Figure 1***.

Featuring this type of conversion capability at the analog front end of PC monitors can be an excellent way to add total system value, as supporting $YP_BP_R$ component inputs ultimately results in an "HD Ready" display set. Moreover, this addition aligns well with the ongoing trend of integrating multimedia functionality to desktop PCs and displays, and could quite possibly provide a second wind for CRT monitors.

National Semiconductor's LMH1251 offers an effective monolithic solution for analog $YP_BP_R$ to RGBHV conversion with superior performance and video quality.

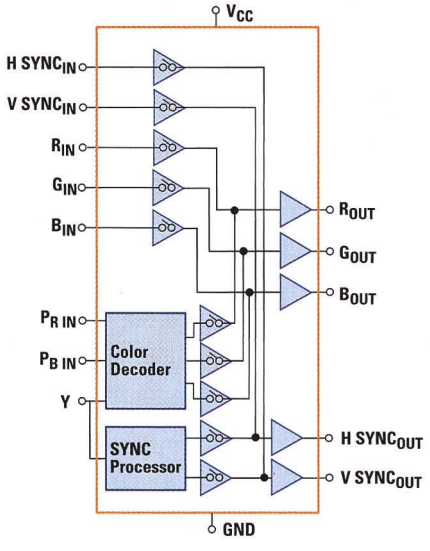
It provides a high performance video multiplexer, which accepts either PC graphics video (RGBHV) or SD/HD video ($YP_BP_R$). This integration of a high bandwidth video switch with a color space dematrixer and sync processor lends itself well for display system architectures, which provides the end user with instant flexibility for viewing HDTV content or PC graphics video at their desktop or projector screen. A simplified block diagram of the LMH1251 is shown in ***Figure 2***.

The high precision analog color decoding within the LMH1251 is carried out in full compliance with the linear equations specified in the EIA/CEA-770.2-C standard for analog component SDTV and the EIA/CEA-770.3-C for analog component HDTV. The highly advanced integrated sync processor is also compatible with the horizontal and vertical timing specifications of these standards. Furthermore, it is fully compatible with Macrovision Corporation's copyright protective sync scheme that is embedded on many DVD movie titles.

A key feature of the LMH1251 device is its capability to automatically detect the incoming component video format. Based on this detection of whether the input is SDTV (480i/480p) or HDTV (720p/1080i), it will then make the decision to apply the appropriate color decoding equation and sync processing scheme. It also provides a status output, specifying the format information, which can be useful to the system MCU. A power save mode feature is included as well, significantly reducing the chip's power consumption during energy save modes, which are common in display systems.

To support high-end PC graphics video input sources as well, the LMH1251 includes a wideband, unity gain RGB video path. With the heightening of PC desktop resolutions that are commonly in use today, the LMH1251 is designed to easily handle modes of up to UXGA (1600x1200), making it ideal for a broad range of display monitors. ■

**Figure 2: Simplified LMH1251 Block Diagram**

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# Featured Products

## Wideband Video Op Amps; Single, Single with Shutdown, and Quad


The LMH6714/20/22 series combine National's VIP10™ high speed complementary bipolar process with National's current feedback topology to produce a very high-speed op amp. These devices offer exceptional performance with a flat gain response of 0.1 dB to 120MHz, a 70 mA continuous output current, and 0.01% and 0.01° differential gain and phase errors for NTSC and PAL video signals. These devices have excellent distortion and bandwidth specifications with low power consumption.

### Features

- 400 MHz (Av = +2V/V, $V_{OUT}$ = 500 $mV_{PP}$) -3 dB BW
- 250 MHz (Av = +2V/V, $V_{OUT}$ = 2 $V_{PP}$) -3 dB BW
- Low power: 5.6 mA/channel
- -70 HD2/-85 HD3 at 5 MHz, 2 $V_{PP}$
- 1800 V/µs slew rate
- Unity gain stable
- Shutdown (LMH6720)
- Low shutdown current: 500 µA (LMH6720)

The LMH6714/20/22 series is ideal for various high-speed applications including video distribution and switching, professional video systems, and wideband active filters. The LMH6714 is available in a SOIC-8 and SOT23-5 package. The LMH6720 is available in a SOIC-8 and SOT23-6 package. The LMH6722 is available in an SOIC-14 package.

**www.national.com/pf/LM/LMH6714.html**
**www.national.com/pf/LM/LMH6720.html**
**www.national.com/pf/LM/LMH6722.html**

## Single/Dual, High-Performance, Low-Power, 8-Bit, 1.5 GSPS (3 GSPS DES mode) A/D Converter

The ADC08D1500 is the industry's lowest power, best performing, dual 8-bit 1.5 GSPS analog-to-digital converter. It digitizes two signals to 8-bit resolution at sampling rates up to 1.7 GSPS or one signal at sampling rates up to 3.4 GSPS. Consuming a typical 1.85W at 3 GSPS from a single 1.9V supply, this device is guaranteed to have no missing codes over the full operating temperature range. The ADC081500 is the single converter conversion of the ADC08D1500.

The unique folding and interpolating architecture, fully differential comparator design, innovative design of the internal sample-and-hold amplifier, and the self-calibration scheme enable a very flat response of all dynamic parameters beyond Nyquist.


### Features

- 7.3 Effective number of bits (ENOB) at Nyquist, 1.5 GSPS (typ.)
- Bit error rate $10^{-18}$ (typ.)
- Interleave mode on the ADC08D1500 for up to 3.4 GSPS sampling
- Choice of SDR or DDR output clocking
- Multiple ADC synchronization capability
- Serial interface for extended control
- Fine adjustment of input full-scale range and offset
- Single +1.9V (±0.1V) operation
- ADC08D1500 Consumes only 1.85W while running at 3 GSPS
- ADC081500 Consumes only 1.2W while running at 1.5 GSPS

The ADC08D1500 and the ADC081500 are well suited for a variety of applications including direct RF down conversion, digital oscilloscopes, satellite set-top boxes, communications systems, and test instrumentation. These converters operate over the Industrial (-40°C ≤ TA ≤+85°C) temperature range and are available in a LQFP-128 package.

**www.national.com/pf/DC/ADC081500.html**
**www.national.com/pf/DC/ADC08D1500.html**

EDITED BY FRAN GRANVILLE

# pulse

INNOVATIONS & INNOVATORS

## Digital imaging makes wafer probing more fun viewing than satellite TV

The eVue digital-imaging system for evaluation-wafer probing adds features that simplify setup, navigation, probing, and data correction.

Targeting use in process-development device-characterization applications, the eVue digital-imaging system from Cascade Microtech offers improved viewing, navigation, and user-friendly features. The system stores images and lets users see close-up details along with images from other parts of a wafer or different zoom levels on the same wafer. Thus, users can see the extended-view "big picture" while they probe. The system automatically optimizes probe-positioning accuracy, measuring-tape functions, and focus.

The eVue Pro software package adds multilevel profile maps and recalls previous data and images for immediate comparison, among other features. The heart of the system, a multi-CCD, wide-field, high-magnification microscope, has both high-definition digital video and three optical paths for multiple-perspective viewing. Prices for the basic eVue system start at $18,999, and the Pro Package sells for $33,999.**—by Bill Schweber**

▷**Cascade Microtech Inc**, www.cascademicrotech.com.

## 0Ω resistor is bridge over troublesome pc-board tracks

A 0Ω crossover jumper may seem like a component solution looking for a problem, but it can solve tricky pc-board-layout problems. One such jumper, the LRZ series from the IRC Advanced Film Division of TT Electronics, has resistance of less than 0.003Ω and inductance of less than 0.2 nH. It targets use in high-current applications, such as power supplies, and can handle maximum currents of 20, 30, or 35A, depending on size. According to Steve Wade, IRC director of sales and marketing, this value is five times the current rating of competitive units on the market. These jumpers are available in conventional 60/40 tin/lead-solder plating or ROHS (reduction-of-hazardous-substances)-compliant versions. Their operating temperature is −65 to +150°C; prices start at 23 cents (1000).


Use the 0Ω LRZ series of crossover jumpers for high-current flyovers, bypassing interfering pc-board tracks.

**—by Bill Schweber**

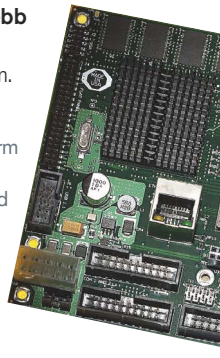
▷**TT Electronics, IRC Advanced Film Division**, www.irctt.com.

## EPIC computer handles shock, vibration, and temperature

Octagon Systems recently announced the XE-700 single-board computer in the new EPIC (embedded-platform-for-industrial-computing) form factor. The XE-700 incorporates the 133-MHz STPC Atlas 5x86-class CPU and targets high-reliability transportation, security, military, and communications applications. Users can boot the module from CompactFlash, and it can operate at a reduced clock rate for lower power operation. It features a 10/100BaseT Ethernet, two USB ports, four RS-232/422/485 serial ports, 24 lines of digital I/O, a video interface, and PC/104 expansion.

The XE-700 withstands 40g shock and 5g vibration and operates in the −40 to +85°C temperature range. Operating-system start-up kits are available for Linux 2.6, QNX, and DOS to enable "instant-on" operation of the XE-700. The single-unit price is $495, and volume discounts are available.**—by Warren Webb**

▷**Octagon Systems**, www.octagonsystems.com.



Based on the new EPIC form factor, Octagon Systems' rugged XE-700 single-board computer operates in the −40 to +85°C temperature range.

# Processor enables integration of high-end control- and data-plane processing

Cavium Networks' Octeon Exp multicore MIPS64-based processor family enables designers to merge control- and data-plane processing at multigigabit/sec rates for enterprise- and storage-networking equipment in one device consuming fewer than 30W. The Octeon Exp offers as many as 16 dual-issue, memory-coherent, MIPS64 Release 2-based cores operating at 600 MHz. The processor architecture includes additional instructions for packet acceleration, and it incorporates a 32-kbyte instruction cache, an 8-kbyte data cache, a 32-entry TLB (translation-look-aside buffer), and a 2-kbyte write-back buffer. The Octeon Exp supports four to eight RGMII (reduced-gigabit media-independent-interface) ports or dual SPI-4.2 interfaces, along with a 64-bit, 133-MHz PCI-X host/slave interface that can act as both data and control interfaces.

To support the throughput requirements for high-performance networking, the Octeon Exp integrates dedicated packet processors for layers 2, 3, and 4 parsing, error checking, tagging, and memory allocation. The Octeon Exp also includes a high-performance, on-chip memory controller that supports 144-bit-wide, ECC-protected DDR II DRAM that operates at an 800-Mbps data rate with capacity as large as 16 Gbytes. Two additional integrated memory interfaces support 18-bit-wide, low-latency RLDRAM (reduced-latency DRAM) 2 and FCRAM (fast-cycle RAM) 2 with low-latency access and a capacity of 1 Gbyte. Designers can use the two memory interfaces to connect TCAMs (ternary-content-addressable memories) for offloading look-ups to an external hardware device. For higher layer data-plane processing, Octeon includes dedicated hardware for TCP acceleration and flow management to scale performance across multiple cores.

The software-programming environment is compatible with C/C++ for MIPS64 and MIPS32 architectures, and it supports the Linux operating system. The Octeon Exp family comprises five devices that are available worldwide without any security-related export-control restrictions. The CN38xx family offers four, eight, 12, or 16 MIPS64-based cores in a footprint-compatible package. Production prices for the CN38xx family range from $350 to $650 (10,000). These devices are available for sampling with software-development support that includes a simulator and reference applications.

**—by Robert Cravotta**

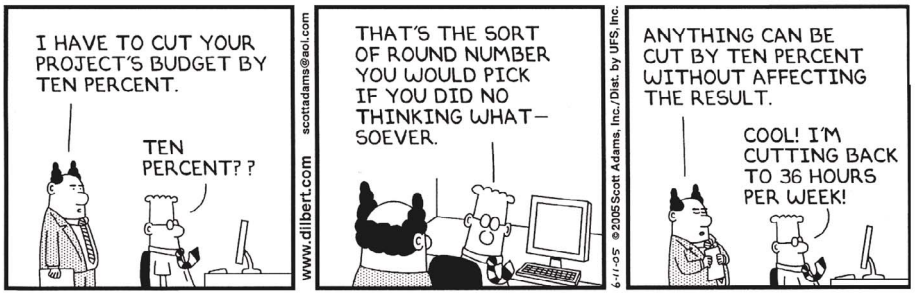
▷**Cavium Networks**, www.caviumnetworks.com.

## FEEDBACK LOOP

**"WHILST (THE SEGWAY) IS UNDOUBTEDLY A REALLY COOL PIECE OF TECHNOLOGY, I ALREADY HAVE A VEHICLE THAT IS CHEAPER, HAS A GREATER MAX SPEED, NEEDS NO ELECTRICITY (IS FUELLED BY CAKE), AND IS LEGAL ON THE ROAD."**

AB Morley, in *EDN*'s Feedback Loop at www.edn.com/article/CA624968. Add your comments.

DILBERT *By Scott Adams*




## 09.15.05

## Actuator uses shape-memory alloy to provide design benefits

**In contrast to conventional electromagnetic, coil-based motors and solenoids, the DM-01 actuator from MIGA Motor Co uses a shape-memory alloy for its prime mover. Suitable for applications such as latch-release mechanisms, vane positioning, robotic motion, and others, the silent unit employs an array of nickel-titanium wires that contract when heated. Actuation time depends on applied input power and is on the order of 25 msec, depending on various current and load factors.**

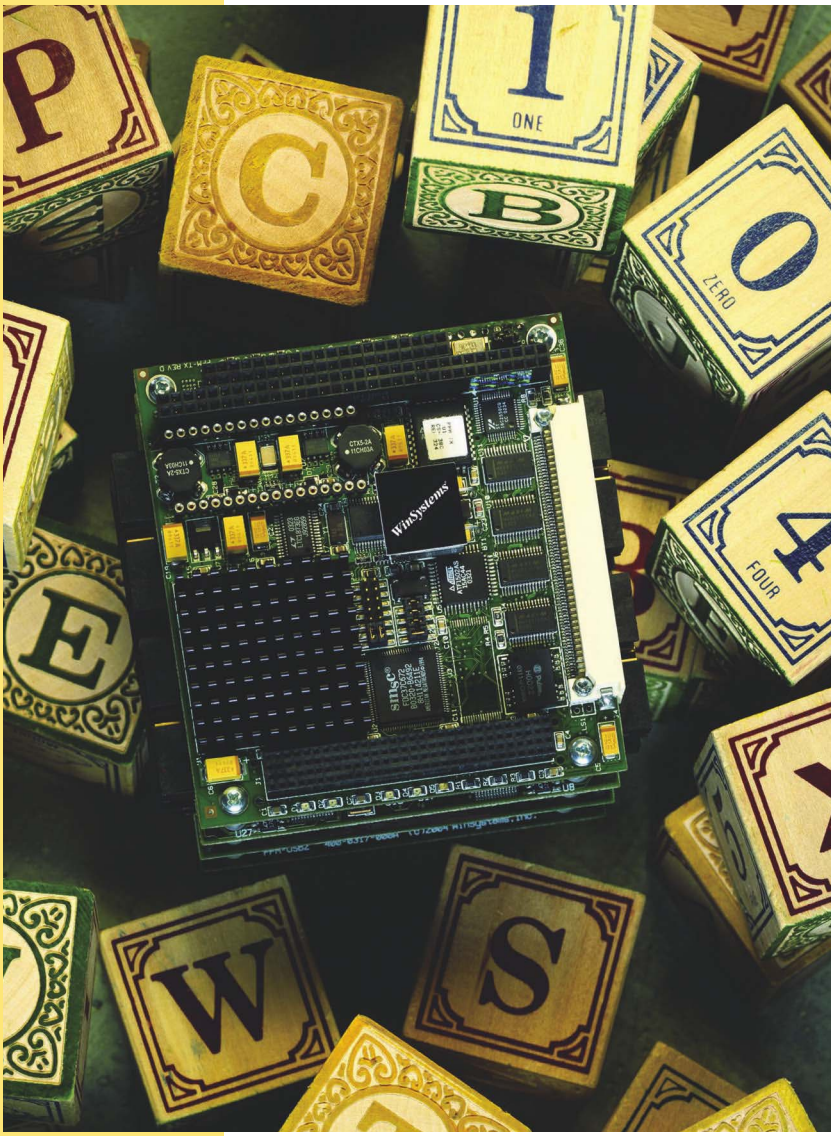
**The device has a 0.5-in. (12.7-mm) stoke and three available output forces of 9 to 20N, depending on model. The 0.7-oz (20g) unit measures about 3×0.7×0.3 in. (76×18×7.5 mm). Current requirements vary with unit force and applied voltage, ranging from 9V at 1.2A to 28V at 9.3A. The DM-01 sells for less than $50 (25).**

**—by Bill Schweber**

▶**MIGA Motor Co, www.migamotors.com.**

The DM-01 uses thermally actuated shape-memory alloys to provide motion in a silent, lightweight package.

# PC/104 Modules: Stackable, Small, and Rugged




Begin your next design with WinSystems' PC/104 and PC/104-*Plus* modules. These compact, 90mm x 96mm (3.6" x 3.8") modules are easy-to-use and ideal for space-sensitive applications.

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  - • USB 2.0
- ▸ Communications
  - • Networking
  - • GSM Cellular
  - • 802.11 Wireless
  - • 10/100/1000Mbps Ethernet
  - • Modem
- ▸ Enclosures
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# Diverse books span wireless-system security, circuit-test sources

Reading a well-organized book that has structure, depth, and breadth is often the most efficient way to learn about a topic or reference a complex subject. One such publication, *Bulletproof Wireless Security: GSM, UMTS, 802.11, and Ad Hoc Security* by Praphul Chandra, is an excellent introduction to a complex subject. Targeting design engineers, this readable, 236-pg book (Newnes/Elsevier, ISBN 0-7506-7746-5) carefully explains the problems of security in various dimensions and begins to address what designers can or should do to enhance security. It examines wireless cryptographic protocols, types of attacks, weaknesses that attacks exploit and how to defend against them, multilayered-security design and protocols, vulnerabilities, and the role of modulation techniques in security. It uses just enough theory to prepare readers but focuses on practical issues and implementations more than the often-challenging math behind message encoding and decoding for secure links.

> Even if you are more likely to buy than build your own, the book explains what you need to look for.

Addressing a far different aspect of the engineering-design spectrum, *Current Sources & Voltage References* by Linden T Harrison thoroughly examines this small but critical area of circuit and IC design. The comprehensive book (Newnes/Elsevier, ISBN-0-7506-7752-X) covers the semiconductor physics, suitable active and passive components and their characteristics, and the circuits that designers build with them. The book dissects and models the various types of FETs, bipolar transistors, and diodes that these circuit functions use and analyzes the resultant performance. These examples use actual devices and model numbers when appropriate. Even if you are more likely to buy than build your own, the book explains what you need to look for when determining the best source or reference for your application.

**—by Bill Schweber**

▷**Newnes/Elsevier**, www.newnespress.com.

# Clock-circuit-design tool recovers engineering time

Analog Devices recently unveiled three clock ICs and a simulation tool that aims to accelerate the design and analysis of clock circuits for various applications, including wireless transceivers, broadband-infrastructure equipment, general instrumentation, and automated test equipment. The ADIsimCLK tool includes tutorials, design wizards, reference designs, a VCO (voltage-controlled-oscillator)/VXO (variable-crystal-oscillator) library, PLL design, loop-filter design, and models.

The tool lets engineers quickly design robust and accurate timing circuits. "This tool allows designers to make design decisions at workstations without hooking up evaluation boards and relying on lengthy data sheets," says Scott Behrhorst, product-marketing manager.

ADIsimCLK addresses several common facets of clock-circuit design, such as speed, edge skew, jitter, and phase noise, as well as less obvious factors, such as external oscillators, slew rate, channel isolation, and RF interference. Analog Devices claims that the tool is the first that can simulate less-than-1-psec jitter and −150-dBc/Hz phase noise. "It lets you predict whether the clock you are using is efficient enough to provide the performance you need," he says. "And it offers comparison interfaces between one clock chip and another through differential LVPECL [low-voltage positive-emitter-coupled logic] for chip-to-chip signaling, which provides indications of what is and is not performing well."

The AD9513, AD9514, and AD9515 clock ICs join devices that the company initially rolled out in December 2004. The new ICs are pin-programmable and offer high integration in small packages, thereby reducing the need for multiple discrete components, saving board space and significantly reducing bill-of-materials costs, according to the company.

The AD9514 and AD9515 support output-clock rates as high as 1.6 GHz, and the AD9513 supports 800 MHz. The AD9513 has three LVDS/CMOS outputs, the AD9514 has two LVPECL outputs and one LVDS/CMOS output, and the AD9515 has one LVPECL output and one LVDS/CMOS output. The ICs come in 32-lead LFSCP packages, feature additive jitter of less than 300 fsec, and can reside close to devices requiring clocks. The devices use their four-level logic pins for programming divide ratios, phase offsets, delays, and output-logic levels, and the ICs require no serial-interface ports.

ADIsimCLK is available for free downloading. The devices are in production. The AD9513 and AD9514 sell for $5.95, and the AD9515 sells for $4.75 (1000).

**—by Jeff Berman**

▷**Analog Devices Inc**, www.adi.com.

## FEEDBACK LOOP

**"THERE IS A SIGNIFICANT DOUBLE STANDARD ON HOW MUCH (SOFTWARE) PIRACY ... COMPANIES ARE WILLING TO LET COUNTRIES AND THEIR 'CULTURES' GET AWAY WITH."**

Frank L, in *EDN*'s Feedback Loop at www.edn.com/article/CA633440. Add your comments.

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# Aircraft ice detector shows sensing challenge, innovation

Sensors measure basic, clearly describable parameters: temperature, pressure, weight, and moisture. However, the reality of an application makes meaningful sensing challenging; hence, an enormous diversity of sensors exists for any given parameter. Demonstrating this dichotomy, the hermetically sealed Model 9732 ice-detecting transducer probe from New Avionics Corp uses a 950-nm laser-diode infrared source and matching detector to assess thickness of ice, based on ice-induced attenuation of the optical path.

Richard Hackmeister, vice president and general manager of the company, says, "We use invisible IR to shine no visible light outside the aircraft, as though it were a running light." The probe, which measures 6 to 8 in. long, depending on version, can detect the first 0.001 in. of ice; the NASA-tested and -calibrated probe can detect ice within 10 sec of entering an icing condition. The support circuitry implements the laser drive, detector-diode interface, and threshold detectors to signal stages of ice growth and has a four-wire interface to the probe itself.

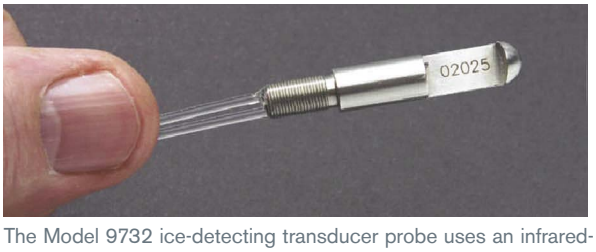
The probe's slim physical shape plus low drag coefficient of 1.09 do not interfere with or affect the onset of an icing condition. This phenomenon occurs when a probe disturbs the airflow, thus slightly warming the local environment, retarding ice development, and leading to a mis-

## Does my measuring instrumentation affect what I am measuring?

leading ice-development assessment. It demonstrates the eternal challenge: "Does my measuring instrumentation affect what I am measuring?" The basic probe tip weighs 0.25 oz, and the complete tip, tube, and shield weigh 3 oz.

Operating from a 3.3V-dc supply at 100 mA or with 200-mA pulses, the device enables engineers to locate the support circuitry as far as 1m from the probe itself. It has no high-speed clocking, so it generates no RFI and withstands ±25g acceleration in all six axes of motion. The unit sells for $799 (50), and the license includes a reference-design schematic, a layout, and a bill of materials.**—by Bill Schweber**

▷**New Avionics Corp**, www.newavionics.com.




The Model 9732 ice-detecting transducer probe uses an infrared-laser diode and collocated photodiode to assess icing conditions, based on optical attenuation in the light path.

# Low-lane-count PCIe switch ventures into new applications

09.15.05

**PLX Technology recently introduced a five-port, eight-lane PCIe (PCI Express) switch for applications such as high-end printers, multichannel network adapters, and notebook docking stations. The PEX 8508 complies with PCI Express Specification R1.1 and offers a reduced footprint and lower power and cost. The PEX 8508 reduces packet latency to less than 150 nsec. The switch features an I²C bus, fatal-error-signal support, ISA/VGA-enabled registers for graphics applications, and four general-purpose I/Os. It can enter an ultralow-power state and wake up via in-band or out-of-band signaling, has hot-plug controllers on all ports, and supports constant frequency and spread-spectrum clocking.**

**The PEX 8508 targets add-in-card applications, such as Ethernet aggregation and processor isolation. "The market for these high-end adapter cards is growing, and it is almost becoming required that these cards have multiple I/Os on them," says John Gudmundson, senior marketing manager.**

**One of the biggest markets for the PEX 8508 is processor isolation. "When isolation processors are on separate cards, there is lower latency," Gudmundson says. "If a board or a processor goes down, you need the other one to quickly take over, and that feature requires low latency through the switch."**

**The PEX 8508 comes in a 19×19-mm, 273-pin PBGA package and will be available for sampling during the fourth quarter. It will cost less than $15 (volume quantities). A rapid-development kit will sell for $995.**

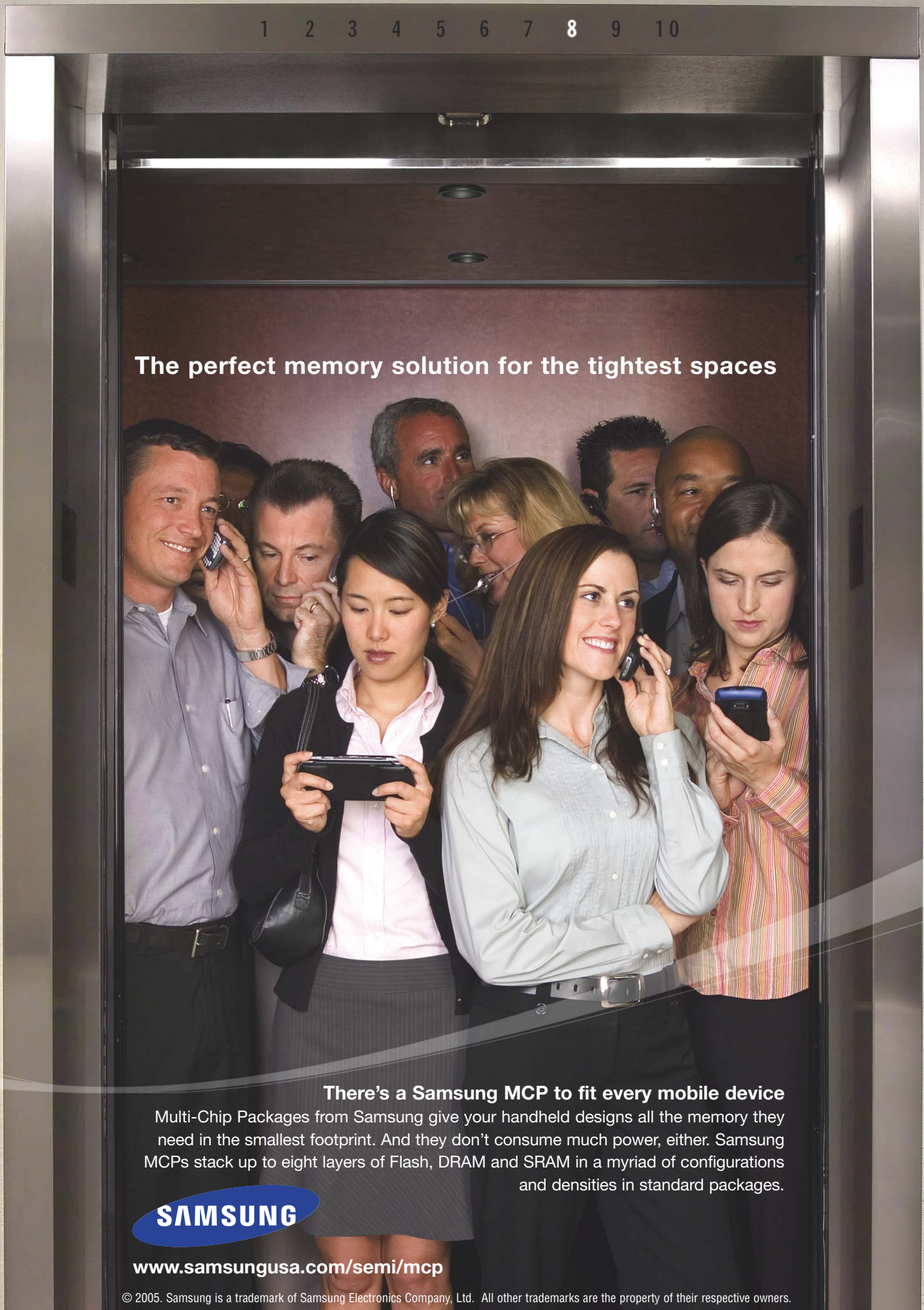
**—by Jeff Berman**

▶**PLX Technology, www.plxtech.com.**

## FEEDBACK LOOP

"SOFTWARE-CONSTRUCTION METHODOLOGY HAS NOT CHANGED IN A FUNDAMENTAL WAY SINCE LADY ADA WROTE THE FIRST ALGORITHMIC PROGRAM FOR BABBAGE'S ANALYTICAL ENGINE, A MACHINE BUILT OUT OF GEARS AND ROTATING SHAFTS! THIS, I BELIEVE, IS WHY SOFTWARE IS SO UNRELIABLE."

Louis Savain, in *EDN*'s Feedback Loop at www.edn.com/article/CA608882. Add your comments.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GLOBAL DESIGNER

# Energy-efficiency standards play a role in external-power-supply design

Energy-conservation organizations issue energy-efficiency standards that can make a difference in external-power-supply design, according to industry executives and energy-conservation organizations. Such organizations include the United States Environmental Protection Agency's Energy Star (www.energystar.gov), the California Energy Commission (www.energy.ca.gov), the European Union (www.europa.eu.int), the Australian Greenhouse Office (www.greenhouse.gov.au), and the China CECP (Certification Center for Energy Conservation Products, www.cecp.org.cn). The organizations are deploying these standards in conjunction with mandatory and voluntary specifications focusing on the efficiency of external power supplies.

"This [proliferation of energy-efficiency standards] is happening on a global level, and there is a move afoot to harmonize global standards for energy conservation for different types of products and adapters," says Doug Bailey, vice president of marketing at Power Integrations, a vendor of high-voltage analog ICs for power conversion.

Although the details of the standards and specifications vary, the underlying objective, according to Energy Star, is to spur the adoption and usage of energy-efficient external power supplies and buoy the concept of deploying a single energy-efficiency-testing procedure and specification for several countries. This model enables designers to compare external power supplies' energy-efficiency outputs and lowers design and production expenses.

This approach is similar to specifications that the CECP issued this year, calling for energy consumption for power-supply components, including cell-phone chargers and adapters, digital cameras, and portable music players. They include minimum operating-efficiency requirements at different output-power levels and a maximum level of no-load power consumption.

According to Andrew Fanara, Energy Star team leader for products, a single global measure to gauge test procedures and energy efficiency of adapters and other components at various power loads and no-load efficiencies allows manufacturers to consistently and fairly compare products and tout efficiencies.

"Our specifications are on the same level as those in other countries," says Fanara. "We would like to make power consumption as low as possible, because there are roughly a billion power supplies and adapters sold worldwide per year."

Although Energy Star has been testing power supplies and adapters, Fanara notes that manufacturers are implementing designs with small, energy-efficient footprints for end users who want to use smaller, less bulky devices with smaller, more efficient power strips. "Designers are focusing more and more on this issue, because more efficient and smaller products bring about more benefits, such as reducing energy bills, for end users," says Fanara. "Designers know that this type of energy efficiency is quickly becoming mandatory."—**by Jeff Berman**

▷**Power Integrations**, www.powerint.com.

09.15.05

## Indian semiconductor companies upgrade engineering skills

Experienced chip designers are becoming an increasingly scarce commodity, as vendors outsource more work to the Indian semiconductor industry. "There is a dearth of design engineers with a combination of electronic-design skills and an adequate knowledge of the latest tools," says G Satish Kumar of Mentor Graphics Sales and Services. To plug the gap, companies such as ATI, Magma, Mentor Graphics, and TI are taking the initiative to upgrade the skills and knowledge of local design engineers. Collectively, the companies spend more than $1 million a year—either in the form of monetary contributions for education or by providing software and tools for design labs in universities. "There is an acute shortage of VLSI front- and back-end-design talent," says Dasaradha R Gude, managing director at ATI Technologies India. Consequently, ATI is collaborating with Hyderbad-based Veda IIT on diploma and master's degree programs for design engineers. "We have trained more than 1000 engineers on the entire Magma flow," comments Anand Anandkumar, managing director of Magma Design Automation India. "Talent that can develop EDA tools and analog ICs is in short supply."

"There is a huge gap between what the universities teach and what the industry requires," confirms Professor K Jayaraman, chief mentor at CICT Pvt Ltd, adding that universities lack the resources for developing labs or to invest in software tools. "The lack of a coordinating body is a problem," says CP Ravikumar, PhD, secretary of the VLSI Society of India. To bridge this divide, the ISA (India Semiconductor Association) and VSA (VLSI Society of India) have launched a pilot program with Belgaum-headquartered VTU (Vishvesvaraya Technological University). "The initiative encompasses research, curriculum, and faculty development, EDA-tool support and ecosystem creation," says Poornima Shenoy, president of ISA. The pilot program will create opportunities for greater industry-academia interaction, create an industry-oriented curriculum, and facilitate the infrastructure to support the programs.—**by Chitra Giridhar,** ***EDN Asia***

▶**ATI Technologies**, www.ati.com.
▶**Magma Design Automation**, www.magma-da.com.
▶**Mentor Graphics**, www.mentor.com.
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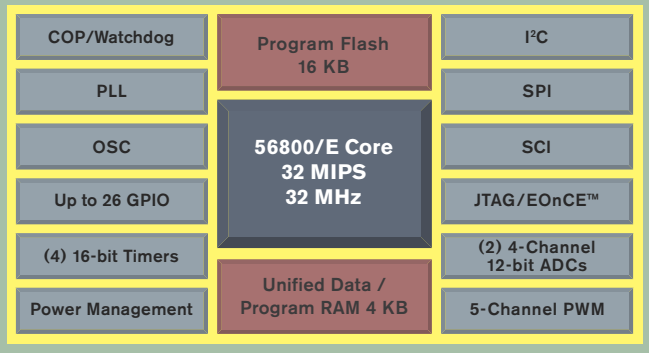


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RESEARCH UPDATE

BY BILL SCHWEBER

# Bendable electronic paper includes image memory

Striving toward the long-sought ideal of the electronic equivalent to conventional paper, Fujitsu Ltd and Fujitsu Laboratories Ltd have demonstrated a film-based, bendable material that displays text and color images and consumes no power when displaying them. Fujitsu officials say that the power to change an image is so low that the weak RF energy in contactless IC cards can deliver that energy to the device.

The substrate material has three layers—for red, green, and blue primary colors—and delivers more vivid images than do standard reflective LCDs, because the material


uses no color filters or polarizing layers. Fujitsu plans to refine and test-market the material, which is suitable for shelf tags, display signage, and flat and curved surfaces, through 2006. You can find details at www.fujitsu.com/global/news/pr/archives/month/2005/20050713-01.html.

▷**Fujitsu Laboratories Ltd**, www.labs.fujitsu.com.

## Laser-enhanced printer gives paper-cutting a new edge

**Researchers at CEA (Commissariat à l'Énergie Atomique) Le Ripault (Monts, France) are giving the standard ink-jet printer a potential role in precise paper-cutting, akin to rapid prototyping, so that users can cut or score invitations, cards, and complicated shapes. The printer assembly combines a conventional print head with a 1W, 810-nm infrared laser diode and an ink that absorbs infrared wavelengths but is transparent to visible light. The company based the ink on pigment from Sigma-Aldrich (www.sigmaaldrich.com).**

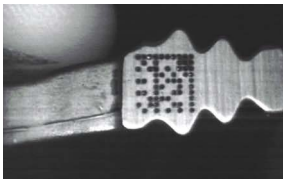
**The printer cuts paper at a speed of less than 1m/minute, far slower than commercial systems, which use kilowatt-range carbon-dioxide lasers and achieve cutting speeds of approximately 1000m/sec. However, the technology is suitable for many desktop applications and low-volume needs. The key to this small-scale system is the recent development of low-cost laser diodes with outputs of 1W at wavelengths of 700 nm and longer. You can find more details at www.cea-technologies.com/article/article.php?article=379.**

**▶Commissariat à l'Énergie Atomique, www.cea.fr.**

09.15.05

## Machine-readable label functions despite obstructions

Manufacturers of complex systems need to mark every part with an ID number, but etched or printed bar codes may not work because they are often covered by paint or



special finishes. To address that problem, researchers at NASA's Marshall Space Flight Center have developed a magnetic-dot-based system with high-magnetic-coercivity ink, in which the dots are "written" in a matrix pattern. This writing can use a stencil or apply the ink in laser-engraved, etched, or machined recesses. A handheld reader senses the matrix pattern, similar to how a bar-code scanner works, and converts the pattern to a standard code-output pattern. The reader can sense the magnetic pattern through as much as 15 mils of paint—typically, five or six layers.

> A handheld reader senses the matrix pattern and converts it to a standard code-output pattern.

The system also has potential in nonaerospace applications, such as automotive production, in which manufacturers paint parts during production or parts become covered with grime and crud in the field, and security, in which vendors can deliberately cover and thus shield the code's existence from prying eyes. You can find more details at http://techtran.msfc.nasa.gov/new/mmrms.html.

▷**NASA**, www.nasa.gov.

## Need the time? NIST can help

Radio-controlled clocks that automatically synchronize to the NIST (National Institute of Standards and Technology) WWVB primary-clock time codes have come down in price, size, and power; you can even get them through specialty stores, such as The Sharper Image.

If you are thinking of incorporating the circuitry into your product, look at the online brochure from NIST WWVB, *Radio Controlled Clocks: Recommended Practices for Manufacturers and Consumers* at http://tf.nist.gov/timefreq/stations/radioclocks.htm. Although some of the advice, such as check the batteries and change the antenna orientation, is obvious, the brochure also offers good insight into the time codes and how your design can use or misuse them, dealing with signal loss, adjusting for Daylight Savings Time, and similar issues.

**▶National Institute of Standards and Technology**, www.nist.gov.

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BY HOWARD JOHNSON, PhD

# Making noise

Friday nights, I play bass in a jazz trio. The sound of my upright acoustic bass easily fills our small club, so I constantly have to think about the level of noise I'm making, and that brings me to the subject of this column.

I recently concluded some power-supply immunity testing on an IC. The test fixture directly injects intentional noise into the power terminal of the DUT (device under test) to see how much it can take without failing.

Ordinarily, I place an impedance in series with the power terminal of the DUT, severely weakening the power system at that point and making it easy to inject substantial quantities of intentional noise into the chip's power terminal. This time a special requirement complicated my test: that the power system feeding the DUT remain unaltered during testing. Making matters even worse, the power system for this layout was hefty. Analysis of the design revealed a power-to-ground impedance of about 0.02Ω at all frequencies as high as 1 GHz.

Pump up the volume with multiple sources.

Under these conditions, to induce ±200 mV of noise on the power plane feeding my DUT, the test apparatus must pump at least ±10A into the power system. To generate that much current, a 50Ω laboratory signal source needs an open-circuit voltage of (10A)×(50Ω)=±500V and dissipates 2500W rms when clamped to $V_{CC}$ by this stiff power system. I've seen bass amps that pump out that much power, but my lab signal source—nor any source I can afford to rent—does not cut it.

How about using a transformer to overcome the mismatch between the source impedance (50Ω) and the load impedance (0.02Ω)? The impedance ratio is 2500-to-1, so a transformer with a 50-to-1 turns ratio should, in theory, reduce the required source current to a level of (±10V)÷(50Ω)=200 mA. The required source voltage would then be (200 mA)×(50Ω)=±10V—an achievable figure. Unfortunately, I was unable to find, or figure out how to construct, any 1-GHz transformer suitable for such a low load impedance. Friday afternoon rolled by, and I still had no way to properly stimulate my system.

**A massive array of sources creates a huge amount of noise.**

Over the weekend, thumbing through the pages of *Bass Player* magazine, I came across a picture of a young woman standing in front of a wall of bass speaker cabinets. Her setup arrayed 32 10-in. speakers in parallel, producing an impregnable wall of sound. That picture triggered a crucial thought in my brain: A massive array of sources creates a huge amount of noise.

My test card now has the DUT on one side, with its power system. On the other side of the card, using a separate power system but shared ground planes, sits a huge FPGA with 400 outputs. Each output pumps noise through a dc blocking capacitor directly onto the $V_{CC}$ plane that the DUT uses. Each FPGA output is programmed as a 50Ω source powered by 3.3V. This circuit easily drives the required ±200 mV onto my DUT power plane. By adjusting the number of active outputs, I control the level of noise.

If you build a similar circuit, don't let it run very long. The source, like good jazz, gets really hot. EDN

*Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com, or e-mail him at howie03@sigcon.com.*

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BY JIM WILLIAMS • LINEAR TECHNOLOGY

# Something from nothing

In the early 1980s, as Linear Technology was just beginning, we had a fundamental problem: products in development but none to sell. But, we wanted prospective customers to know our name and what we were up to. Our public-relations company glibly urged "controlling the press" and "getting our message out" but offered little real substance.

This approach seemed arrogant folly, and I felt a restless, uneasy malaise. We couldn't and shouldn't control the press; we should feed it what it wants. Editors aren't fools. They value what interests their readers. Going to them with puffery and hype would be self-defeating. The real issue was finding a way to productively use the seeming dead time before product availability. What *EDN*'s editors and their readers wanted was a series of credible, full-length technical articles in the language of relevant, working circuits.

I moped for weeks over this problem before a possible solution became apparent. Instead of waiting for products, I'd simply go into the lab, develop the applications, and then write the articles. The key to this approach was to synthesize the expected products using available ICs and discretes to build rough equivalents on small plug-in boards. We could develop functional applications and write most of the text. We'd then shelve the manuscript and breadboards. Later, when products became available, we could put them into the breadboards and implement the attendant final changes. Once we had done these tasks, we could drop scope photos and specifications into the waiting text, tweak the manuscript, and ship it off to *EDN*. This approach would speed publication by perhaps a year and synchronize the article's appearance with product introduction.

Initially, the whole scheme appeared absurd and eminently unworkable, with uncountable technical and editorial sinkholes. Getting started was much more difficult than I had imagined. Synthesizing the hardware for our unborn ICs proved tricky; my methods, clumsy and stumbling. Breadboarding the applications was laborious and slow, primarily because I wasn't sure how accurately I was mimicking the forthcoming IC's performance. Writing was equally painful. Text flow was staccato and disjointed because of the gaps that occurred while I waited for results with actual products. I had to keep separate notes directing me to unfinished text when we finally dropped the products into the breadboards.

The first article took almost two months, but things slowly became easier. Tricks to move along the lab work evolved, and I found ways to write more efficiently, making the manuscripts inherently adaptable to the planned additions and changes. Soon, I was producing an almost-finished article every two weeks or so, roaring along, powered by adrenaline, solder, pencils, paper, and pizza.

During the next year, life was a dizzy seven-day-a-week blur of breadboards and manuscripts shuttling between work and my home lab. My diet was a cardiologist's nightmare. I don't recall having a meal at home. The refrigerator was devoid of food but well-provisioned with Polaroid film to feed the oscilloscope camera. All this frenetic bustle boiled off any semblance of a normal social life. At dinner in San Francisco, while nominally listening to my date describe her job intricacies, I silently calculated the optimum chopper-channel crossover frequency in a composite amplifier. This regimen of madness continued for about a year, resulting in 35 full-length feature articles appearing in *EDN* between June 1983 and November 1987.

I still write for *EDN*, although at a significantly less frenetic pace. Now, when the kids in our lab complain to me about writing technical material, I try not to sound like the curmudgeon I am not so slowly becoming. I think that mad tear almost 25 years ago contributes to my current lack of empathy. These kids today, with a catalog full of products, they don't know what they've got.

*Long-time* EDN *contributor Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), has more than 20 years' experience in analog-circuit and instrumentation design. Like Jim, you can share your tale. E-mail mgwright@edn.com.*

DANIEL VASCONCELLOS

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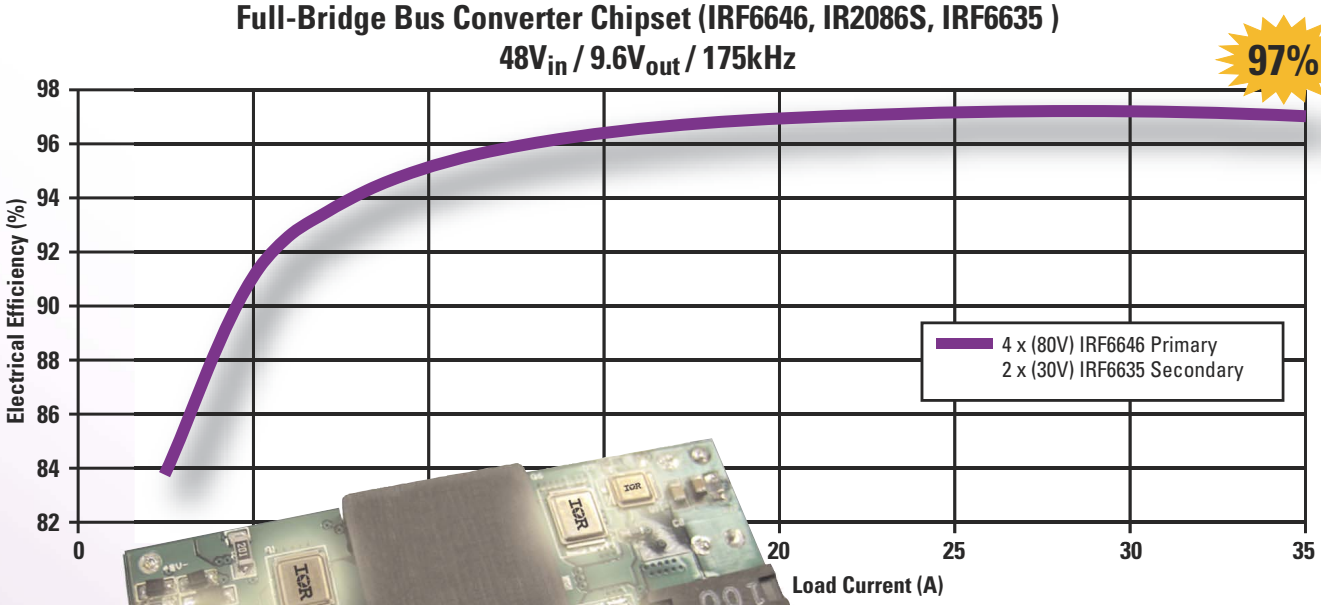
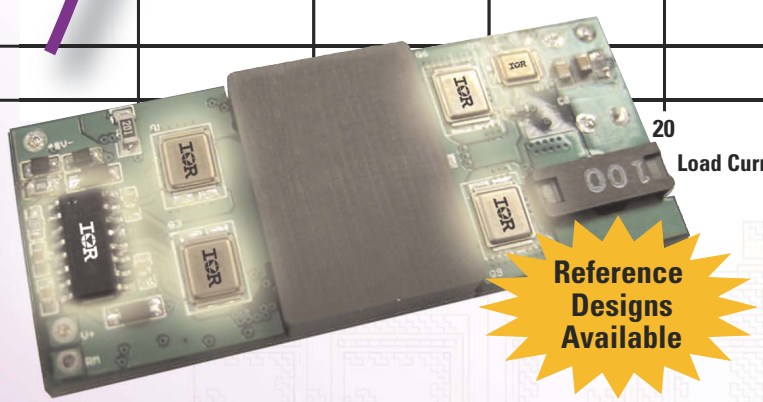
**$48V_{in}$ / $9.6V_{out}$ / 175kHz**




**New DC-DC Chipset Solution from International Rectifier**

| DirectFET™ MOSFETs | | | | | |
|---|---|---|---|---|---|
| Part # | Package | $V_{DSS}$ | $R_{DS(on)}$ max @ $V_{GS}$=10V | $Q_G$ Typical | $Q_{GD}$ Typical |
| IRF6644 | Medium can | 100V | 13mΩ | 35nC | 11.5nC |
| IRF6655 | Small can | 100V | 62mΩ | 8.7nC | 2.8nC |
| ★ IRF6646 | Medium can | 80V | 9.5mΩ | 36nC | 12nC |
| IRF6613 | Medium can | 40V | 3.4mΩ | 42nC | 12.6nC |
| IRF6614 | Small can | 40V | 8.3mΩ | 19nC | 6.0nC |
| ★ IRF6635 | Medium can | 30V | 1.8mΩ | 47nC | 17nC |

| Control IC | | | |
|---|---|---|---|
| Part # | Package | Voltage Rating | Description |
| IR2085S | SO-8 | 100V | Primary-side half-bridge control IC, fixed 50% duty cycle, self-oscillating |
| ★ IR2086S | SO-16 | 100V | Primary-side full-bridge control IC, fixed 50% duty cycle, self-oscillating |

★ – IR product featured in Full-Bridge Bus Converter reference design above



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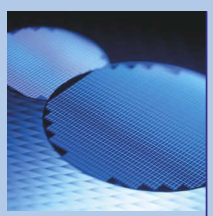

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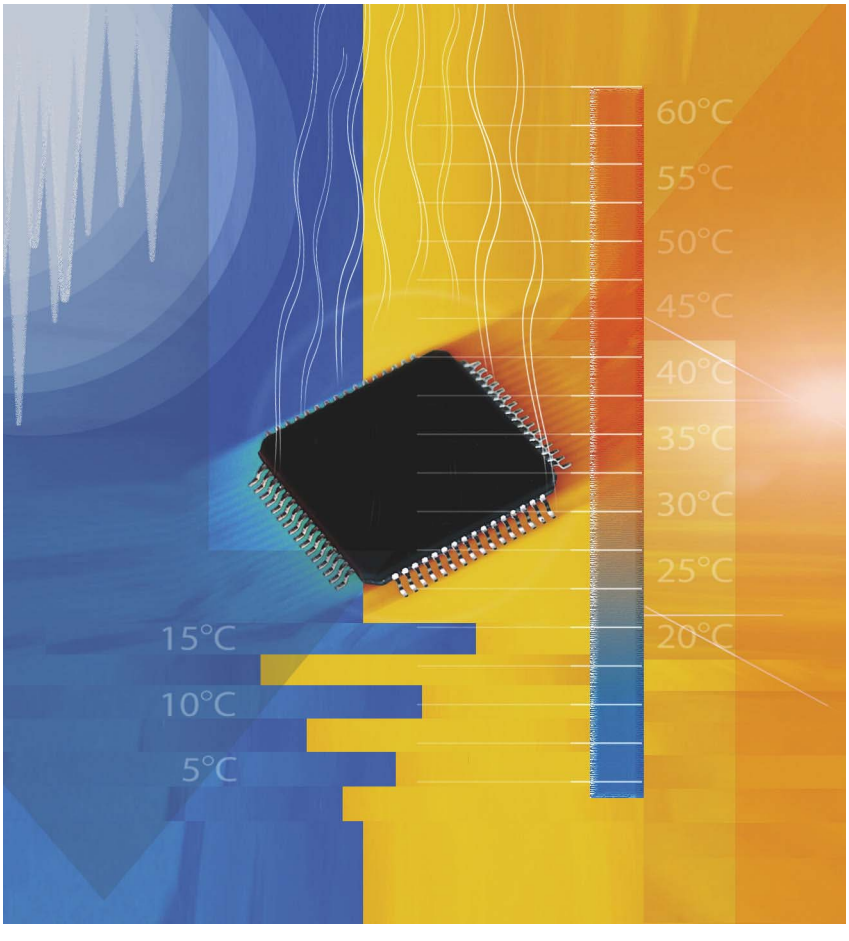
[1] iSuppli, 2005 and Gartner Dataquest, 2004

BY MICHAEL SANTARINI • SENIOR EDITOR

# Thermal integrity: a must for low-power-IC digital design

THIS YEAR'S DESIGN AUTOMATION CONFERENCE HAD NO SHORTAGE OF ESTABLISHED VENDORS AND START-UPS INTRODUCING POWER TOOLS PURPORTING TO GIVE DIGITAL-IC DESIGNERS A BETTER WAY TO ESTIMATE POWER.




Over the last three years, IC-power management has moved from a third-order to a first-order concern for chip designers, especially those designing ASICs and SOCs (systems on chips) for portable-system applications. Accordingly, many power tools made their debut at this year's Design Automation Conference, which took place in Anaheim, CA, in June. Experts say that, to get a true grasp of transistor leakage—an ever-larger consumer of system power—you must first get a read on the thermal effects of your design and how they impact the timing and reliability of digital ICs. Experts assert that, if you get an accurate account of heat on your chip, you can maximize your design for the right mix of power, performance, and reliability.

If you're designing at process geometries of 90 or even 130 nm, you know that IC-power management is a big problem. Several EDA companies have developed tools to estimate active power, which is power a system consumes through normal operation and computing. Some vendors have also developed tools that try to account for leakage power, which leaks from transistors when systems are in standby mode. Leakage was a problem at the 130-nm node and has become a huge problem as designs moved into 90 and 65 nm. Experts say that designers cannot account for leakage and, thus, IC-power consumption without accurate thermal analysis.

"As temperature increases, leakage increases exponentially," says Andrew Yang, president and chief executive officer of Apache Design Solutions. "TSMC [Taiwan Semiconductor Manufacturing Co] projects that leakage consumes about 50% of the total power. We've asked our customers implementing designs on 90-nm silicon, and they are seeing that leakage consumes 25 to 40% of power. In moving to 65 nm, we expect 50 to 70% of total power will be lost through leakage." A lot of that leakage results from inaccurate estimates of temperature, and

## AT A GLANCE

- Leakage power exponentially increases with temperature.
- At 90-nm-process nodes, leakage accounts for 25 to 40% of total power. At 65-nm processes, leakage accounts for 50 to 70% of total power.
- On-chip temperature impacts timing. Every 15°C increase causes delay of approximately 10 to 15%.
- EM increases exponentially with temperature increases and reduces the life of products by four times.
- Resistance is a linear function of temperature, affecting IR drop. A change of 15°C increases resistance by 10%.
- Clock gating and multithreshold CMOS increase on-chip thermal variation.

most of that inaccuracy is due to the use of outdated maximum-temperature limitations and models passed to package and systems designers.

Rajit Chandra, president and chief executive officer of Gradient Design Automation, says that temperature has always to some extent been a factor in IC design, but, for the most part, designers targeting thermal tolerance have based their work on the fact that the temperature on the IC should not exceed 105°C. For more than a decade, that rule has dominated. But, as designs target finer process geometries and designers place more functions on a chip, designing to 105°C across the chip is not the most effective route for hitting performance goals, and vendors are working toward a lower maximum temperature.

Transmeta is one such company. It offers the LongRun2 low-power-design methodology to fabs. The company's founder and chief technology officer, Dave Ditzel, a noted processor designer, says that IC-design groups today often make power-versus-performance trade-offs. "Because leakage is such a big issue, people who used to spec parts at 105°C are targeting lower maximum temperatures," he says. "If you look at a typical desktop CPU, it will likely be rated for only 85°C. To control leakage, people would like to even further reduce that temperature." Library vendors and fabs all offer low-power processes, low-thermal-voltage transistors, and multithreshold CMOS, but Ditzel says users give up clock speed when going to those structures.

Chandra says that many of today's SOCs are so large and perform so many functions that areas of the die develop microclimates and hot spots instead of maintaining a constant and predictable temperature across the die (**Figure 1**). "Reality starts diverging from traditional assumptions regarding temperature in ICs," says Chandra. "For example, if you assume your chip to be 25°C and it is actually 35°C in a spot on the chip where there are low-thermal-voltage transistors that are leaking, then the current will go up by 50%. With the next 10°C rise in temperature, the current will go up 126%." If you take it a step further and assume that the chip runs at 25°C and it is actually running at 45°C, then, according to Chandra, "You will be way off on power and even timing on a bunch of transistors." Add ambient heat from the climate to the mix, and the problem gets worse. "Unlike the old days, when you asked what the average power was, and temperature was just an afterthought, temperature is now driving the power," he says.

Yang and Chandra say that popular low-power-management techniques of clock gating and power gating, shutting down parts of the design when not in use, can be the main culprits in creating localized hot spots or microclimates. "To reduce power, people use clock gating, essentially shutting down certain clock domains, reducing certain parts and activity of the design and cooling them," says Yang. "In fine-grained clock gating, we see a temperature variation on chip as opposed to having everything toggle in a statistical way. Power gating through the use of multithreshold CMOS to deliberately shut down parts also causes on-chip temperature variation." He says that everything on an IC should simultaneously heat up and cool down, but that situation doesn't occur in fine-grained devices. "Having portions of a design heat up while other portions of the design cool down can cause race conditions in extreme cases or hold-time and matching violations, similar to what analog designers have dealt with for years," says Yang. He predicts that thermal impact on low-power design will become more important as chip designers start to use clock- and power-gating design techniques.

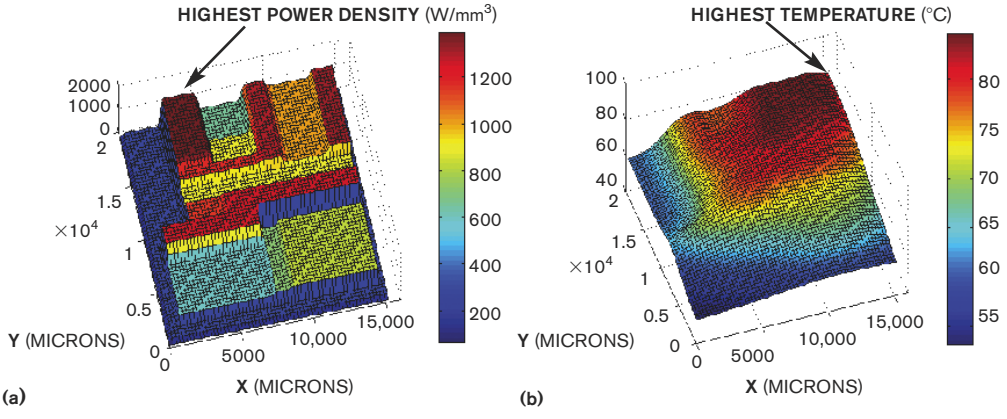



Figure 1 Heat can migrate on an IC. The section of an IC with the highest power density (a) is not always the hottest area of the IC (b).

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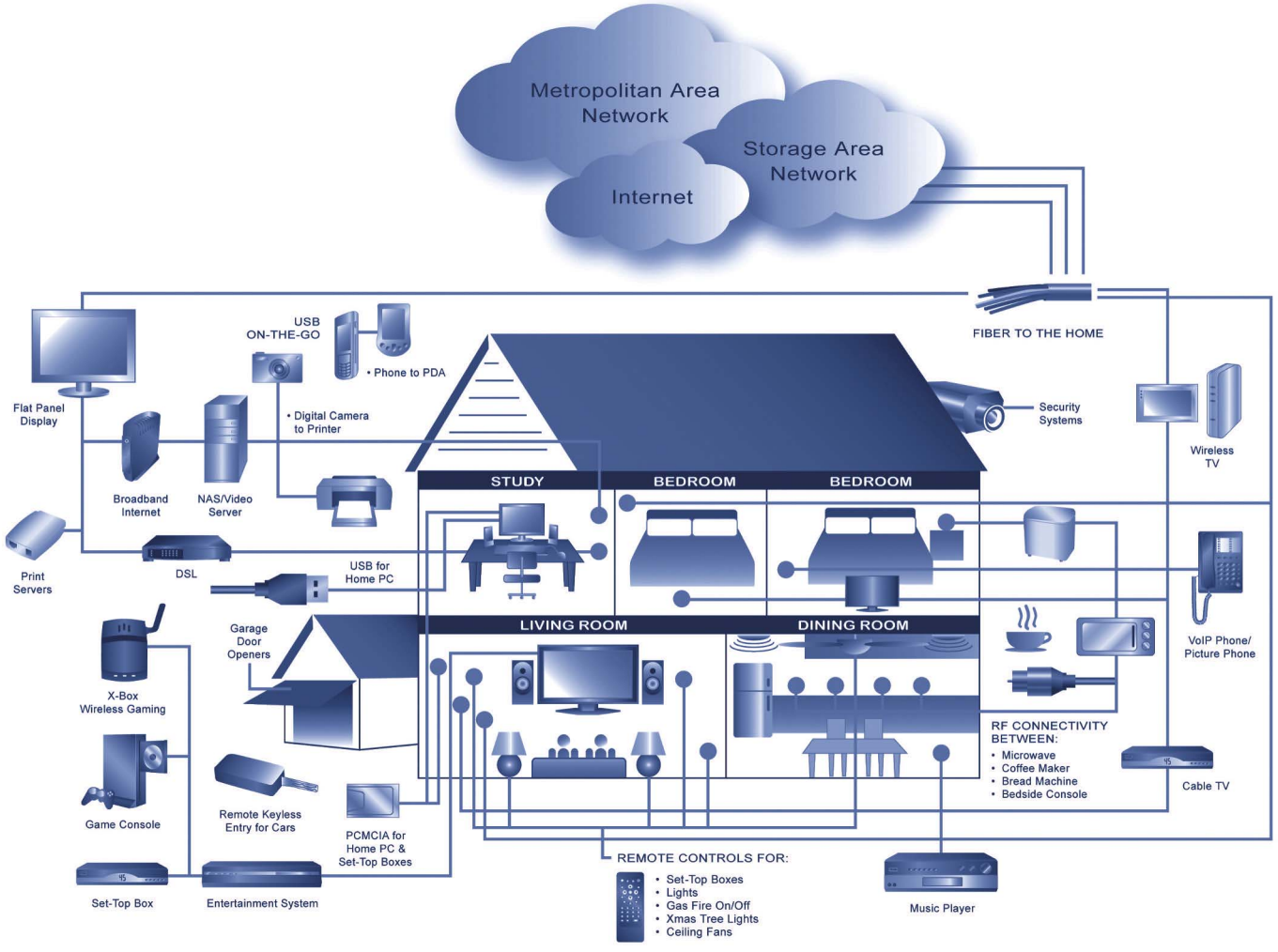


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On the other hand, Transmeta's Ditzel thinks that microclimates are insignificant problems in designs using a 90-nm process. "You get variation as dies get bigger, but that evens out quickly over time," he says.

## THERMAL IMPACT

When performing thermal analysis, designers have to also consider power leakage, on-chip temperature, reliability, electromigration, and IR drop. "Clock timing is sensitive to temperature variation," says Yang. "Every 15°C increase locally causes a delay or slew to increase roughly 10 to 15% locally. So, a temperature increase does slow things down." Electromigration also increases exponentially with increases in temperature. "Typically, a chip has a maximum tolerance of 105°C, but, if the local area heats up 15°C, the chance of electromigration increases exponentially, reducing the lifetime of a device by four times," he says. He notes, too, that resistance scales linearly with temperature, so, for a 10 to 15°C increase in temperature, resistance of the local area increases by 10%. As a result, IR drop increases by about 10%, according to Yang.

Traditionally, vendors have relegated the job of cooling ICs to package and system designers. But experts argue that the package-design step occurs too late in the process and that package designers typically have insufficiently accurate thermal estimates to build the optimum package for a part. "Package designers have traditionally been given just one temperature to work with," says Chandra. "The package designers think they can completely cool off the entire chip, but that assumption is incorrect. The energy devices, like the leaking devices and critical paths, continue to generate heat. Package design will reduce some—but not all—of the temperature."

Designing a package with too low a thermal tolerance can be costly because it can lead to overheating and failure of the chips, whereas excessive use of guardbands; extravagant packages; and extravagant cooling schemes, such as employing on-package fans, can add expense to projects. In the 90-nm era, package designers need more accurate power and thermal data from IC designers. Inaccurate power analysis can lead to power variation across a wafer. "As you go to higher performance devices, you find that not all parts leak the same," says Ditzel. He points out that the die on a wafer have varying degrees of performance and power consumption.

The power grade and, thus, heat vary by as much as a factor of four across a wafer. "Faster parts are those with lower threshold voltages. They also are the parts with the highest leakage," Ditzel says. "In that case, your power estimate, expressed in $CV^2f$ [total switched capacitance times the power-supply voltage squared times the switching frequency], is the same, but you have a huge variation in leakage," he says. "It has to do with statistical variation in processing: The fab can control the threshold voltage only so well, so it has some variations. That variation can greatly affect your design." This variation may be acceptable for microprocessor vendors that have many products in various speed and power versions. However, SOC and ASIC vendors having to meet certain performance and power specs cannot tolerate that variation. For ASIC designers, the device either meets performance requirements or ends up in the trash. The variation across the wafer also leads to a problem for package designers if they receive a spec with a lower-than-needed maximum-temperature specification.

Chandra proposes eliminating the wall between the chip and package designers. "Because of the temperature issues and the regional effect of heat, leakage has in many ways caused people to think about packaging, heat sinks, and thermal gradients within the chip," he says. "They all need to come together to better serve chip cost-effectiveness and chip quality." He notes that companies such as Ansoft and Flomerics offer tools that analyze electromechanical issues and junction and ambient temperature. "Those vendors are traditionally not concerned about how power changes with temperature and how it distributes itself

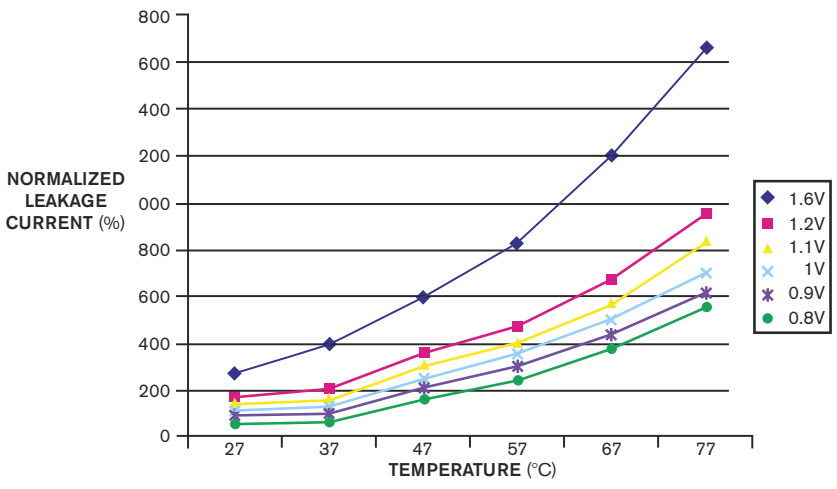


Figure 2 Leakage current and hence leakage power decreases with decreasing $V_{DD}$ but increases exponentially with temperature. For this test case, leakage values were observed with a $V_{DD}$ of 1V and a temperature of 27°C.

**TABLE 1 TEMPERATURE-IMPACT AREAS**

| | Analog designs | Digital processors | Mobile designs | Automotive applications |
|---|---|---|---|---|
| Temperature gradient and sensitivity | X | | | X |
| Power and delay | | X | X | X |
| Electromigration and MTBF | | X | X | X |
| Battery life | X | | X | |

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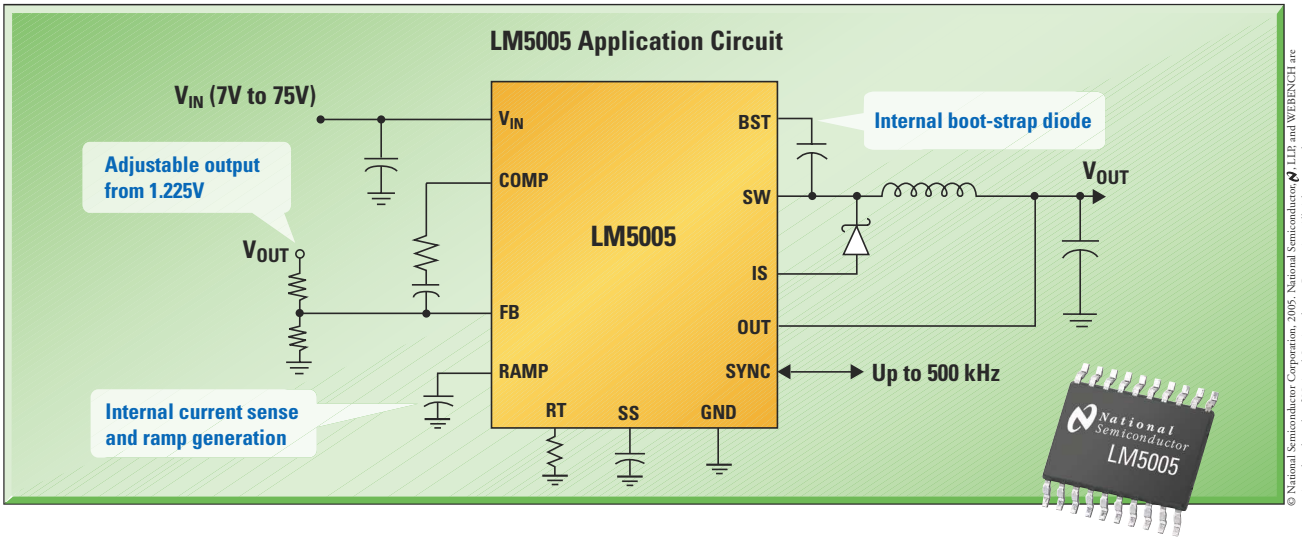




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| LM5007 | 9V to 75V input, 500 mA step-down | Up to 800 kHz | ✔ | — | ✔ | MSOP-8, LLP-8 |
| LM5008 | 9V to 100V input, 350 mA step-down | Up to 800 kHz | ✔ | — | ✔ | MSOP-8, LLP-8 |
| LM5010 | 8V to 75V input, 1A step-down | Up to 1 MHz | ✔ | ✔ | ✔ | TSSOP-14, LLP-10 |


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within a chip," Chandra says, noting that vendors in that area may soon work more closely with EDA companies.

## THERMAL-INTEGRITY ANALYSIS

Yang and Chandra predict that thermal analysis will become a hot area in software tools and that designers must account for thermal effects if they want to home in on the right mix of leakage, performance, reliability, and package. "First, there was signal integrity; then, there was power integrity; now, the next analysis we will need to do is thermal integrity," says Yang. His company, Apache Design, which beat by three years most of the flock of EDA vendors into power-integrity analysis, currently offers no thermal-analysis tools but is considering adding them. Yang envisions that a comprehensive thermal-integrity flow will evolve in which users first perform active- and leakage-power estimations and then perform thermal simulation. "Thermal simulation will take in the package and process parameters—for example, the thermal resistance of the package, the heat sink, and the substrate information—and simulate the thermal-resistance and -capacitance networks to derive a steady-state temperature," he says. "The key is the feedback between power and thermal simulation. If you are not careful, you can get a thermal-runaway condition."

After thermal simulation, users will develop an on-chip thermal profile to analyze the power and thermal impact on chip timing, reliability, IR drop, dynamic-voltage drop, and ground bounce. "We can't analyze those conditions using worst-case, steady-state temperature throughout the whole design," says Yang. "They cannot consider the variation effects." He says that, after analysis, users will give the information to package designers and apply the information to IC layouts. "Users will move blocks around to avoid localized temperature buildup or, in some cases, widen wires to reduce current density and self-heating," says Yang.

Gradient, which introduced its FireBolt thermal-analysis tool at DAC, has a trademark on the term "thermal integrity." Gradient's stand-alone tool performs an on-chip thermal analysis and locates hot spots. The company also has patented on-chip heat-sink structures that designers can add to the metal layers in instances in which conventional layout fixes don't work (**Table 1**). According to the company, the thin substrate of silicon-on-insulator and strained silicon is highly susceptible to on-chip thermal variation. Low-k dielectrics have poor thermal conductivity that traps heat in wires (**Figure 2**).

Other than Gradient, Magma is the only other tool vendor now offering customers digital-IC-thermal-analysis tools, which it has integrated in its Blast-Rail and Blast-Rail 5.0 products. The tools use a scalable polynomial-leakage model to get an accurate reading of on-chip temperature variation. Users identify hot spots at full-chip level and perform more thorough analysis after the tools identify hot spots. "In the early stages of the flow, you don't want to characterize each cell, but, as the design progresses, you want to characterize critical cells, such as those in the critical path," says Amir Ajami, consulting staff member at Magma. "Those paths get the most use, and that means they generate the most heat. They also have the biggest impact on the general distribution of the overall clock signals."

**AS THE DESIGN PROGRESSES, YOU WANT TO CHARACTERIZE CRITICAL CELLS, SUCH AS THOSE IN THE CRITICAL PATH.**

## FIXING THERMALS

Designers can employ a number of techniques to correct thermal-related problems. "One trick is simply to move design blocks around and equalize temperature across the chip during floorplanning," says Chandra. Designers can also make wires more robust and reduce leakage by widening traces and using low-thermal-voltage transistors. However, this approach slows performance and increases area. The method is an effective way to reduce leakage and prevent electromigration. To fix problems with nonuniform power consumption and to get a more constant temperature, users can adjust buffer sizing and placements.

Academic researchers are testing the use of dummy vias in the higher metal layers to reduce nonuniform temperatures on interconnect without impacting resistance and capacitance. "If you insert dummy vias at certain locations along the global line, you reduce the distance between the interconnect and the substrate, reducing the length and cooling the line faster because the substrate will work like a heat sink," said Ajami. "It reduces the impact of the gradient on the interconnect."

Transmeta also claims that its LongRun2 helps ease the power-management problem. "It makes it easy to control the threshold voltages of devices," says Ditzel. The company offers a tool kit that helps them to implement dynamic threshold-voltage control to get the right level of performance when systems are running and in standby mode. EDN

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For a related article, go to www.edn.com/article/CA607747.

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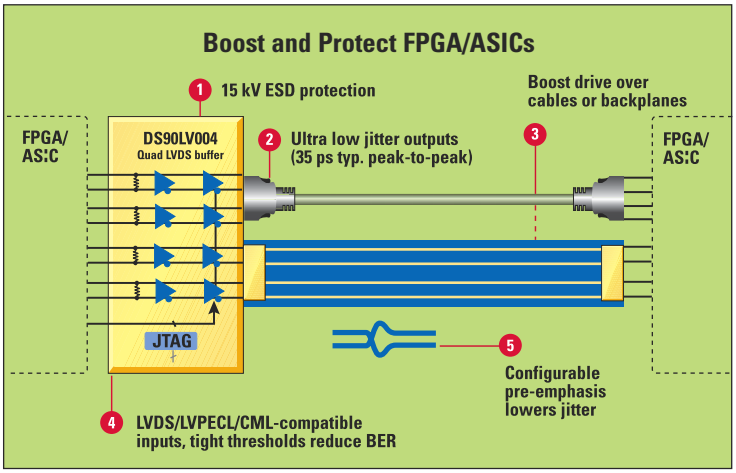


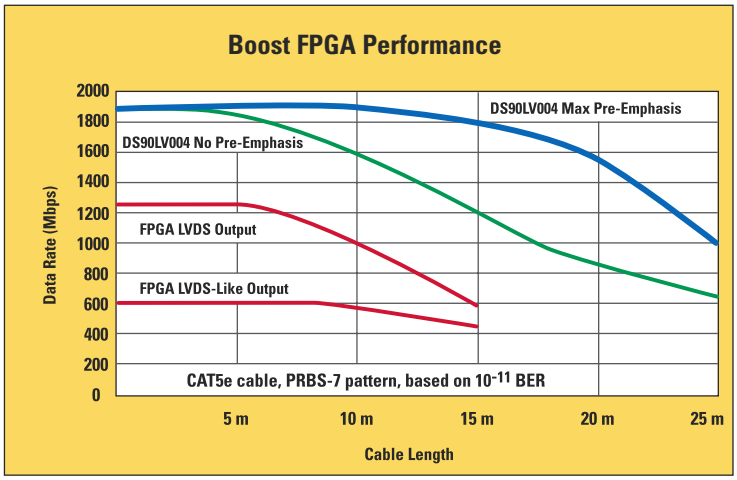




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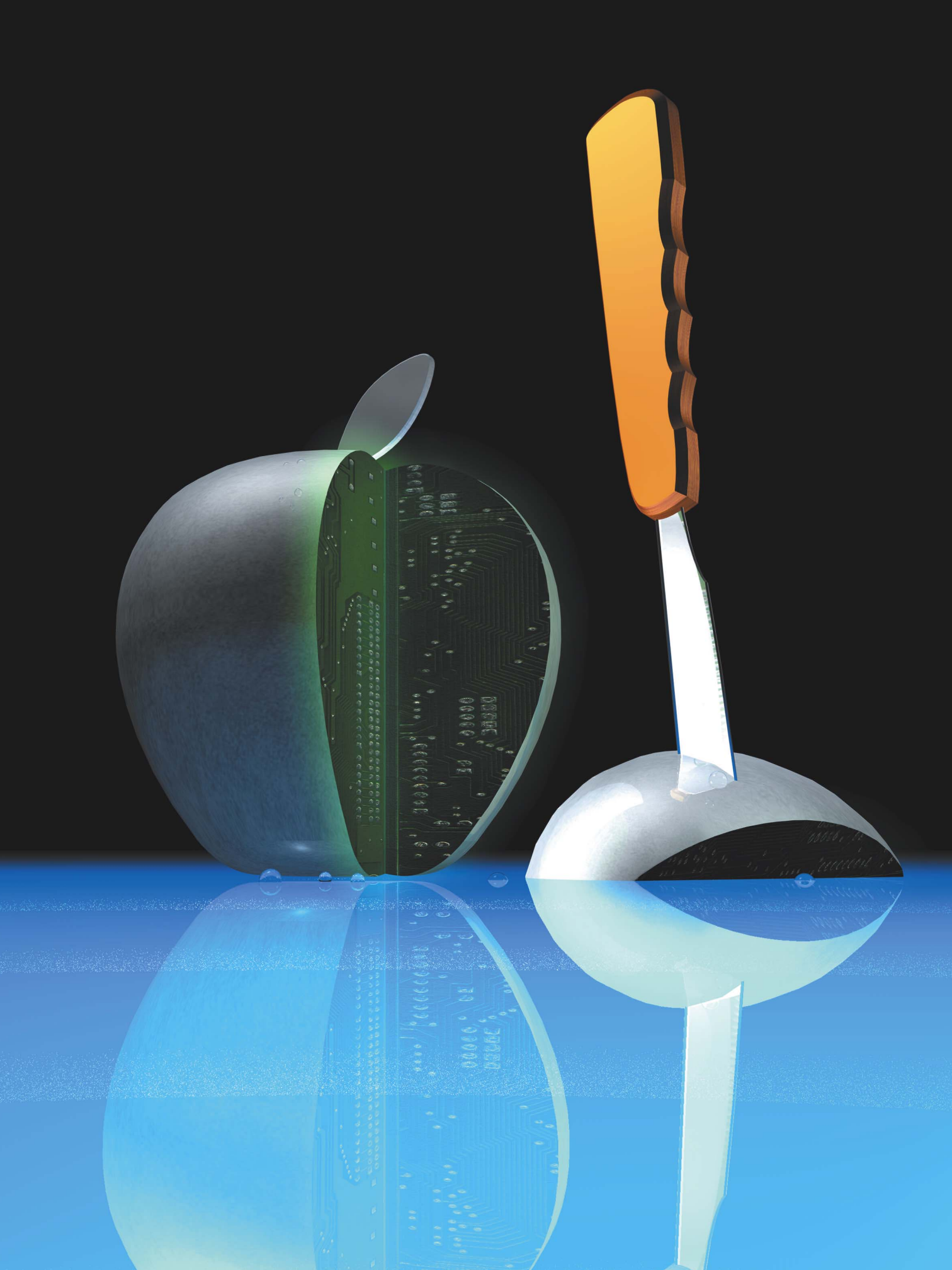

APPLE'S DROPPING THE POWERPC AND MOVING TO X86. MICROSOFT'S DROPPING X86 AND MOVING TO THE POWERPC, JOINING NINTENDO AND SONY. WHICH COMPANY IS RIGHT, OR ARE THEY ALL RIGHT? AND WHAT'S THE BEST CHOICE FOR *YOUR* DESIGN?

BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR

**Go to www.edn.com/050915cs for tables that detail all of the benchmarking data.**

# Mac (under) the knife:

## piecing together the PowerPC puzzle

Three notable events in the high-tech industry so far this year have particularly influenced the status of the PowerPC CPU in embedded-system applications and the broader electronics market. Beginning in mid-March, IBM published a series of articles promoting the Apple Mac Mini as an embedded hardware- and software-development platform, both under the Mac OS and with various iterations of Linux and BSD Unix (**references 1** and **2**; see **sidebar** "Linux: a work in progress"). In mid-May, all three next-generation game consoles (Microsoft's Xbox 360, Nintendo's Revolution, and Sony's PlayStation 3), containing various spins of the PowerPC architecture, went public at the E3 Expo. And, in early June, Apple Chief Executive Officer Steve Jobs announced that the company would begin a phased transition away from the PowerPC to Intel x86 CPUs (**references 3** and **4**; see **sidebar** "New PowerPC flavors").

The diverging game-console-versus-computer trends have provoked a vigorous cyberspace and water-cooler debate regarding the future of the PowerPC, both absolutely and relative to its chief 32- and 64-bit competitor, the x86. Is the Mac Mini, as IBM's documentation claims, a valid development vehicle for PowerPC-based embedded-system designs? What does next-generation game-console developers' embrace of the PowerPC architecture indicate about its cost, performance, power consumption, and other attributes? And, conversely, does Apple's embrace of x86 suggest that the PowerPC is at a crossroads compared with AMD-, Intel-, and Via-supplied CPU alternatives? These are some of the questions that the development efforts, benchmark results, and other issues raised and resolved in this hands-on project attempt to explore.

### THE HARDWARE

Following the recommendations outlined in IBM's literature, *EDN* purchased a 1.25-GHz Mac Mini, with the SuperDrive writable-DVD-drive option, for $553 after rebate (**Table 1**). Stay tuned for a product teardown in a future *EDN* Prying Eyes section. The Mac Mini's specifications are similar to those of a PowerBook that's also in the *EDN* computer pool, giving credence to the oft-

## AT A GLANCE

- Recent events put an added twist on the long-standing x86-versus-PowerPC debate.
- Four hardware platforms, along with multiple subsystem combinations for one of them, give numerous data points for a more complete picture.
- SPEC data is, for now, integer-specific and does not reflect multiprocessor presence.
- Xbench testing provides highly detailed results, some of which are not readily explainable.
- The project lives on; keep an eye out for future print articles and blog postings.

touted observation that (simplistically speaking) Apple repackaged an iBook laptop and removed the LCD from it to come up with the Mac Mini (**Figure 1**). The 32-bit G4 (PowerPC 74xx) CPUs in both systems run at 1.25 GHz, with a 167-MHz FSB (front-side-bus) frequency and no L3 cache. The core clock speed of the CPUs in the Mac Mini and PowerBook exceeds that of many PowerPC-based embedded designs. To give the project additional relevance to *EDN* readers, therefore, we also acquired a four-year-old G4 Power Mac through a winning bid on an Ebay auction.

The dual 800-MHz G4 Power Mac system (code-named Quicksilver) showcased in this article has half the L2 cache of its Mac Mini and Powerbook G4-based counterparts but contains 2 Mbytes' worth of off-CPU L3 cache consisting of synchronous SRAM running at one-quarter the core CPU-clock rate. The cost-slimming L3-cache omission on the Mac Mini and PowerBook is perhaps more understandable when you realize that their SDRAM runs at a higher peak data rate than the L3 cache in the dual G4 Power Mac can support! This first-generation Quicksilver system, which runs its single-data-rate SDRAM at a PC100 speed setting, also came in 733- and 867-MHz single-CPU variants; second-generation Quicksilver systems delivered 800- and 933-MHz (single-CPU) and 1-GHz (dual-CPU) speeds and underwent a minor L3-cache evolution, switching to DDR (double-data-rate) SRAM that ran at half the CPU core clock speed. Follow-on "Mirrored Drive Door" systems marked the end of the line for the G4 Power Mac series; they further evolved the memory subsystem by switching from SDRAM to DDR SDRAM.

This project also harnessed a dual 1.8-GHz G5 Power Mac, at the other end of the performance spectrum from the dual G4 Power Mac. This second-generation iteration of the platform includes PCI slots along with a four-DIMM architecture; the first-generation dual 1.8-GHz G5 Power Mac supported PCI-X add-in cards and included six DDR SDRAM slots. This system's FSB speed is half the core clock frequency (in this case, 900 MHz), whereas the single-CPU 1.8-GHz G5 Power Mac ran the FSB at one-third the core clock rate, presumably to maximize the test yield for the CPU and other system components. The G5 (PowerPC 970FX) CPU supports 64-bit addresses and data, in contrast to its 32-bit G4 predecessor, as well as a full-duplex FSB. Other enhancements include a larger, faster L1-cache subsystem, faster L2 cache (as with the Mac Mini and PowerBook, not supplemented by costly L3 cache), DDR400 SDRAM, and dual SATA drives in a RAID (redundant-array-of-independent-drives) 1 configuration.

Version 4.2.0a15 of Apple's CHUD (Computer Hardware Understanding Development) tools allows the user to disable nap mode on the PowerPC CPU. (We disabled nap mode for all of the benchmarks in this project.) On the G4 systems, it can also disable the L2 cache. Previous versions of CHUD reportedly could also disable the L3 cache in the G4 Power Mac, but Version 4.2.0a15 appears to


Figure 1 Apple's 1.25-MHz Mac Mini (a), 1.25-GHz G4 PowerBook (b), dual 800-MHz G4 Quicksilver Power Mac with GeeThree's Sweet Multiport installed (c), and dual 1.8-GHz G5 Power Mac (d) underwent intensive benchmark scrutiny during this hands-on project.

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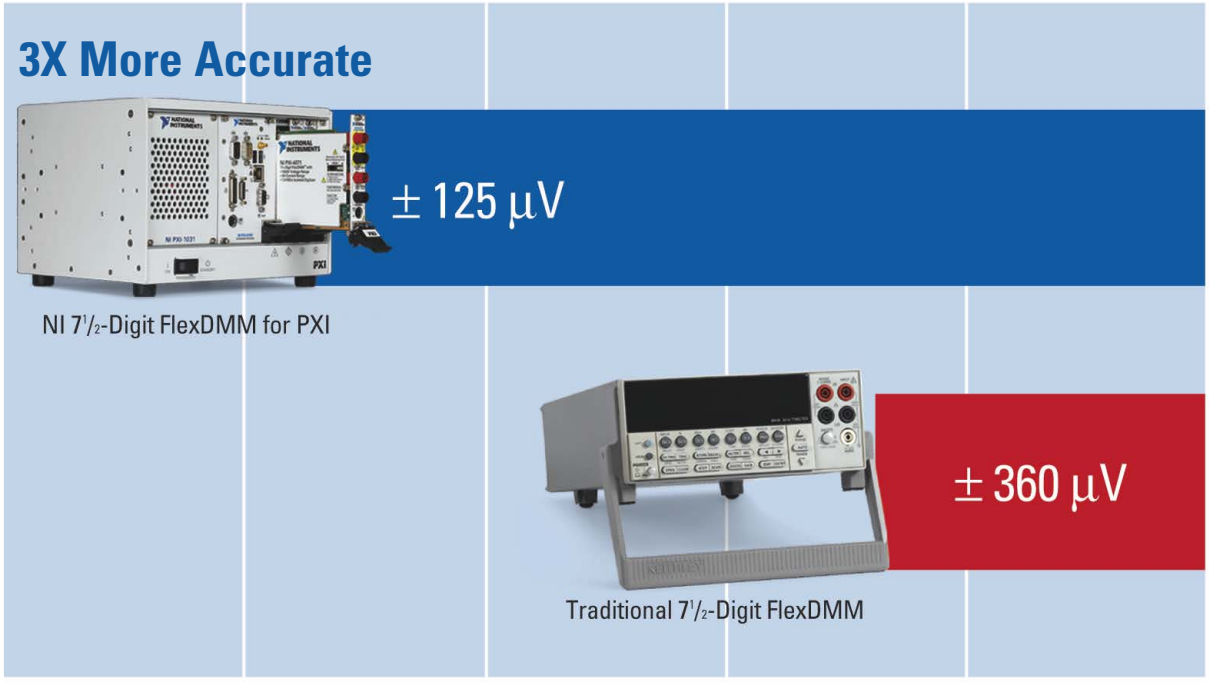


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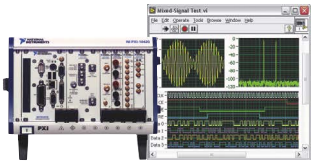

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**TABLE 1 SYSTEM SPECIFICATIONS**

| | G4 Mac Mini | G4 PowerBook | Dual G4 Power Mac (Quicksilver) | Dual G5 Power Mac |
|---|---|---|---|---|
| Processors | 1.25-GHz PowerPC 7447A Version 1.2 | 1.25-GHz PowerPC 7457 Version 1.1 | Two 800-MHz PowerPC 7450 Version 2.1 | Two 1.8-GHz PowerPC 970FX Version 3.0 |
| Front-side bus | 167 MHz (32-bit, half-duplex) | 167 MHz (32-bit, half-duplex) | 133 MHz (32-bit, half-duplex) | 900 MHz (64-bit, full-duplex) |
| L1 cache | 32-kbyte instruction and 32-kbyte data, 1.25 GHz | 32-kbyte instruction and 32-kbyte data, 1.25 GHz | 32-kbyte instruction and 32-kbyte data (per processor), 800 MHz | 64-kbyte instruction and 32-kbyte data (per processor), 1.8 GHz |
| L2 cache | 512 kbyte, 1.25 GHz | 512 kbyte, 1.25 GHz | 256 kbyte (per processor), 800 MHz | 512 kbyte (per processor), 1.8 GHz |
| L3 cache | NA | NA | 2 Mbyte (unified), 200 MHz | NA |
| DRAM | 128-Mbyte (Nanya), 256-Mbyte (Hynix), and 1-Gbyte (Micron) DDR400 CL3 SDRAM, and 512-Mbyte (Samsung) DDR333 CL2.5 SDRAM (all run at DDR333 CL2.5 speeds in-system) | 1.5-Gbyte DDR333 CL2.5 SDRAM (one 1-Gbyte SoDIMM from Kingston and one 512-Mbyte SoDIMM from Samsung) | 1.5-Gbyte PC-133 SDRAM (one 512-Mbyte DIMM from Hynix and two 512-Mbyte DIMMs from Samsung) | 3-Gbyte DDR400 CL3 SDRAM (two 512-Mbyte DIMMs from Corsair and two 1-Gbyte DIMMs from Samsung) |
| Hard-disk drive | 100-Gbyte Seagate 4200-rpm and 5400-rpm, 2.5-in. PATA, both with 8-Mbyte cache | 80-Gbyte Hitachi 4200-rpm 2.5-in. PATA, 2-Mbyte cache | 40-Gbyte IBM 7200-rpm 3.5-in. PATA-100, 2-Mbyte cache | Two 250-Gbyte Maxtor 7200-rpm, 3.5-in. SATA-150, one with 8-Mbyte cache and the other with 16-Mbyte cache, RAID 1 configuration using SoftRAID |
| Graphics | 32-Mbyte AGP ATI Radeon 9200 | 64-Mbyte AGP ATI Mobility Radeon 9600 | 32-Mbyte AGP Nvidia GeForce2 MX | 128-Mbyte AGP ATI Radeon 9600XT |

eliminate this feature. With both the dual-core G4 and G5 Power Macs, CHUD additionally allows the user to disable the second microprocessor. This project's benchmarking exploited CHUD's configuration capabilities to more fully understand the variables that influence perceived system performance. Disabling the L2 cache also potentially enables the CPUs to more closely mimic the performance of reduced-cache and no-cache embedded PowerPC processors from AMCC, Freescale, and IBM, along with CPU cores from these companies and from Xilinx's Virtex-II Pro FPGAs (see **sidebar**, "Embedding the Mac Mini").

The Mac Mini's published specifications include a 4200-rpm, 2.5-in. hard-disk drive and PC2700 (DDR333) CL2.5 (CAS, column address strobe, latency=2.5 clocks) SDRAM. Yet, when the system arrived, its System Profiler report revealed a 5400-rpm Seagate Momentus hard-disk drive, along with PC3200 (DDR400) CL3 (CAS latency=three clocks) SDRAM. Initial Mac Mini user feedback included complaints about slow system performance believed to be the fault of the low-speed hard-disk drive, and it's possible that Apple has decided to spend the extra money for 5400-rpm drives to address those concerns. *EDN* ran benchmarks using both 4200- and 5400-rpm Momentus drives to quantify any system-performance differences between them, employing Bombich Software's Carbon Copy Cloner utility, along with an ADS Technologies' external hard-disk-drive enclosure, to make a mirror image of the in-system drive before doing the drive swap.

Other Mac Mini user-performance grumbles centered on the 256 Mbytes of system memory in the base configuration, so *EDN*'s benchmarks tested system-memory capacities of 128 Mbytes to 1 Gbyte. Apple's public-relations contacts confirmed that the DDR400 memory would run at DDR333 speeds in the Mac Mini and that its presence versus DDR333 simply reflected relative market availability and cost at the time of its manufacture. Apple's second-generation Mac Minis, introduced at press time, bumped up the base-system memory to 512 Mbytes at no incremental cost, so there likely was some truth to users' complaints with first-generation units. Both the hard-disk drive and memory replacements done in conjunction with this project required opening the Mac Mini's

## CRACKING OPEN THE CASE

**Gaining access to the guts of the Mac Mini isn't *too* difficult, once you obtain the proper tool. It's a putty knife with a paper-thin blade, believe it or not, and the official Apple service manual even documents it. Insert the putty-knife-blade edge in the gap between the bottom assembly and each side of the metal housing, bend it backward to spring loose the internal latches, and don't fear the gruesome-sounding popping noises that result.**

**For a more detailed explanation (additional research is *highly* recommended before you proceed), search the Internet using keyword "mac_mini.pdf" for the Apple service manual. Other World Computing offers a QuickTime video clip of the procedure at http://eshop.macsales.com/shop/mac-mini at multiple resolutions. And PB FixIt offers a number of disassembly, parts-replacement, and reassembly instruction guides in PDF format at www.pbfixit.com/Guide/82.0.0.html.**

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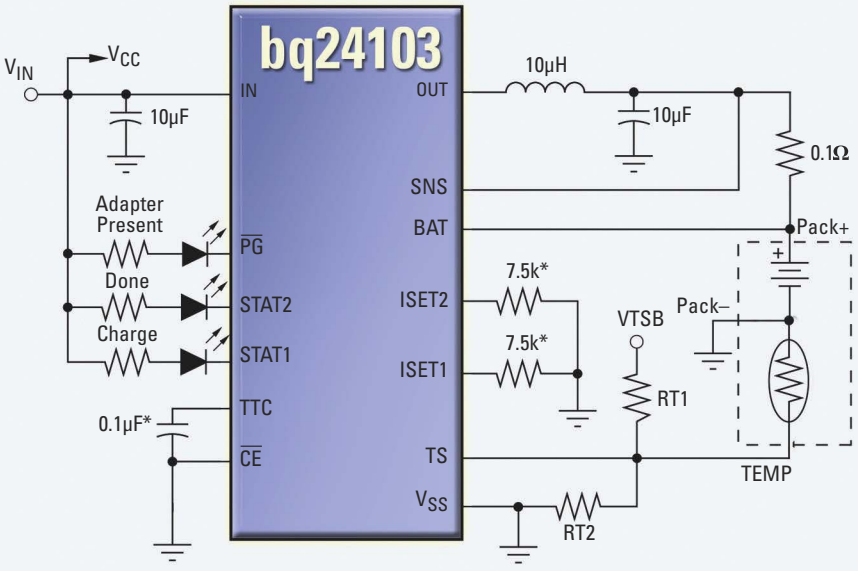


*$I_{Charge}$ = 1.33A, $I_{Precharge}$ = 0.13A, Timer = 260 min

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enclosure, which wasn't a simple feat (**sidebar** "Cracking open the case").

## SOFTWARE AND BENCHMARKS

All four systems showcased in this project ran OS 10.3.9 (code-named Panther). However, the latest Version 2.1 of Apple's free Xcode development tools, whose integrated GCC (GNU C compiler, http://gcc.gnu.org) Version 4 we used to compile the SPEC (Standard Performance Evaluation Corp) benchmarks, runs only under OS 10.4 (Tiger). Therefore, code compilation took place on a separate 15-in. PowerBook owned by Eric Nedervold, a veteran Mac OS- and Java-application developer, who also participated in the project.

Xbench (www.xbench.com), a well-known Mac-system-benchmarking utility, tests numerous computer subsystems and generates detailed reports of its findings. This project used Version 1.1.3 of Xbench, which was released in late 2003. Version 1.2, which was also released just as this article went to press, focused on OS 10.4 support as well as compatibility with Mac development systems based on Intel CPUs; neither issue affects this project's parameters. However, because Xbench is a Mac-only program, you cannot directly compare its results with benchmarks run on x86-based systems.

Therefore, this project also encompasses SPEC CPU2000 Version 1.2 benchmarks, which are by design platform-independent. The SPEC Web site reveals an abundance of published SPEC CPU2000 results spanning multiple CPU architectures, including AMD and Intel x86, Intel Itanium, Hewlett-Packard PA-RISC, Sun Microsystems SPARC, and MIPS. But the only PowerPC results it lists are from IBM, and they come from workstations and servers. Mac-based results are notably absent from the list, and this project fills in some of the missing pieces. SPEC benchmarking on the Mac Mini employed a system configuration with 1 Gbyte of system memory and a 5400-rpm hard-disk drive.

As their name implies, SPECINT (integer) benchmarks test integer performance, and they're based on the C and C++ (for the 252.eon function) languages. (See **Table 2** at www.edn.com/050915cs.) The SPECINT suite includes the following functions:

- 164.gzip (reference-time-1400) data-compression utility;
- 175.vpr (reference-time-1400) FPGA circuit-placement and routing;
- 176.gcc (reference-time-1100) C compiler;
- 181.mcf (reference-time-1800) minimum-cost network-flow solver;
- 186.crafty (reference-time-1000) chess program;
- 197.parser (reference-time-1800) natural-language processing;
- 252.eon (reference-time-1300) ray tracing;
- 253.perlbmk (reference-time-1800) Perl;
- 254.gap (reference-time-1100) computational-group theory;
- 255.vortex (reference-time-1900) object-oriented database;
- 256.bzip2 (reference-time-1500) data-compression utility; and
- 300.twolf (reference-time-3000) place-and-route simulator.

Within a single benchmark session, each function ran three times, and the SPEC software used the median score in its report. (Rather than average the three scores, it simply selects the middle one.) SPECFP (floating point) contains 14 floating-point-intensive functions, written in a combination of Fortran-77 (six functions), Fortran-90 (four), and C (four) languages:

- 168.wupwise (reference-time-1600) quantum chromodynamics;

## LINUX: A WORK IN PROGRESS

**Taking our cue from IBM's Mac Mini documentation, we installed Terra Soft Solutions' YDL (Yellow Dog Linux) 4.01 on the system on a previously blank 60-Gbyte hard-disk drive. Unfortunately, we didn't get far in our evaluation. We knew that YDL 4.01 wouldn't support the Mac Mini's built-in sound chip or the Broadcom-based WiFi (Wireless Fidelity) transceiver in the integrated wireless module. (That drawback was one of the reasons we didn't spend $100 extra on this option.) However, one of the primary enhancements of the YDL Version 4.01 over the Version 4.0 predecessor was supposed to be full support for the Mac Mini's more-than-two-year-old ATI Radeon 9200 GPU (graphics-processing unit).**

**Postinstallation, the Mac Mini came up in a graphics mode in which roughly 20% of the screen, including the all-important Linux equivalent of the "start" button and program icons, shifted left off the visible desktop. (The Mac Mini was connected to a Compaq TFT5030 display.) Redefining the display from a generic monitor to a generic 1024×768-pixel LCD, we obtained a relatively stable 640×480-pixel GUI, but higher resolutions were unavailable. The display would still occasionally come up in a stretched and left-shifted mode, but exiting and re-entering X-Windows or, in the worst case, rebooting Linux, would fix it. Attempts to explicitly identify the GPU as a Radeon 9200, therefore using a device-specific graphics driver instead of the default generic driver, resulted in a garbled, illegible output akin to a system's driving a progressive-scan display with an interlaced video signal.**

**In response to the display problem, Terra Soft's Chief Executive Officer Kai Staat comments, "The Mac Mini has a funky graphics card that is not easy to work with." The system would also randomly boot up with the built-in Ethernet adapter disabled. We also tried to directly run the Live DVD version of Ubuntu Linux (www.ubuntulinux.org) Version 5.04 and had even less success; the system reset to an open-firmware prompt and froze when we selected the G4-specific build. When we selected the PowerPC generic Ubuntu variant, it complained about the GPU's frame buffer and refused to load X-Windows. Linux on the Mac Mini, we reluctantly conclude, remains not ready for prime time, except perhaps for the operating system's core constituency of patient power users.**


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- 171.swim (reference-time-3100) shallow-water modeling;
- 172.mgrid (reference-time-1800) multigrid solver in a 3-D potential field;
- 173.applu (reference-time-2100) parabolic and elliptic partial differential equations;
- 177.mesa (reference-time-1400) 3-D-graphics library;
- 178.galgel (reference-time-2900) fluid dynamics (analysis of oscillatory instability);
- 179.art (reference-time-2600) neural-network simulation (adaptive resonance theory);
- 183.equake (reference-time-1300) finite-element simulation; earthquake modeling;
- 187.facerec (reference-time-1900) computer vision (facial recognition);
- 188.ammp (reference-time-2200) computational chemistry;
- 189.lucas (reference-time-2000) number theory (primality testing);
- 191.fma3d (reference-time-2100) finite-element crash simulation;
- 200.sixtrack (reference-time-1100) particle-accelerator model; and
- 301.apsi (reference-time-2600) problem solving regarding temperature, wind, velocity, and the distribution of pollutants.

Unfortunately, Xcode does not include a Fortran compiler, so this article does not include SPECFP results. Our first stab at compiling the SPECINT routines comprehended two GCC PowerPC-generic speed-tailored optimizations: "O0" (for no optimization) and "O3" (for full optimization). We ran into problems compiling the "eon" routine that a type mismatch in the header files caused. After more than a week of stop-and-go debugging, we created G4- and G5-optimized compilations, after surmounting even more compiler-versus-code incompatibilities.

Keep this information in mind as you peruse the following data and especially when comparing our results with those on the SPEC Web site. We're not compiler experts, and it's highly conceivable that by fine-tuning the compiler flags, a power user *might* be able to squeeze a few more percentage points' worth of performance out of some or all of these chips. (Note that the SPEC license agreement expressly forbids altering *any* of the routines' source code.) Keep in mind, too, that both the SPEC and the Xbench routines ran on systems with full OS X images loaded—not a stripped-down, text-only-mode Darwin configuration. Specifically, the dual G4 Power Mac, dual G5 Power Mac, and Mac Mini were all running Redstone Software's OSXVNC server utility, which, according to OS X's Activity Monitor, added a virtually undetectable incremental load to the system. We did terminate or otherwise disable all unnecessary background functions, however.

## EMBEDDING THE MAC MINI

**Does IBM's vision of the Mac Mini as an embedded-development platform hold water? This simple question has a complex answer. Keep in mind, first, that the G4 PowerPC CPU in the Mac Mini has an excess of features compared with most embedded-PowerPC variants; examples include its out-of-order code-execution support, its abundant on-chip cache, and its AltiVec SIMD (single-instruction multiple-data) instruction set. Your code performance profile may differ greatly under the G4 than with the CPU in your final design, even if they run at comparable clock speeds.**

**Apple achieved the Mac Mini's compact size at the expense of expansion capability. There's no industry-standard PCI or equivalent bus connector into which you can plug add-in boards; the developer note provides some information on the inner workings of the system, but Apple doesn't detail the pinout and timings of the connector that mates up with the optional Bluetooth-and-WiFi (Wireless Fidelity) mezzanine board (Reference A). This dearth of internal expansion also means, for example, that you're stuck with the ATI Radeon 9200 graphics chip, and that you can bump up the system's main memory capacity to only whatever fits on a single DDR SDRAM DIMM.**

**With respect to external expansion, the Mac Mini supports only FireWire 400–not FireWire 800. You'll also find only 10/100-Mbit Ethernet support; there's no Gigabit Ethernet capability. And, turning your attention to software, the sidebar "Linux: a work in progress" details the difficulty we had getting Linux to run on the Mac Mini, specifically with respect to the graphics subsystem. Linux-distribution providers will clean up such glitches over time, but they're likely to occur with other operating systems, as well.**

**What about the next step: taking the Mac Mini directly to production as the hardware foundation for your system design? The allure of a fully debugged, high-volume production board, especially one that in its base configuration costs less than $500, is compelling. But as a recently published iSuppli teardown report suggests, you'll be supporting Apple's profit aspirations; iSuppli estimated the bill-of-materials cost for the entry-level Mac Mini at $274.69 ($283.37 including manufacturing costs, Reference B).**

**Part of what you're paying for–the Mac OS X operating system and iLife application suite that come with the Mac Mini–you probably won't even end up using. The Mac Mini system board isn't in any sort of an industry-standard form factor (unless you count the fact that it snugly and, likely, coincidentally slips into the single-DIN slot of an automobile sound system). And you'll be subject to the rapid obsolescence-and-replacement cycles of the PC business; don't assume you'll be able to buy the same Mac Mini configuration or, frankly, for that matter, *any* Mac Mini a few years down the road.**


**REFERENCES**

**A http://developer.apple.com/documentation/Hardware/Developer_Notes/Macintosh_CPUs-G4/MacMiniG4.**

**B www.isupply.com/marketwatch/default.asp?id=311.**

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# POWERpuzzler #6

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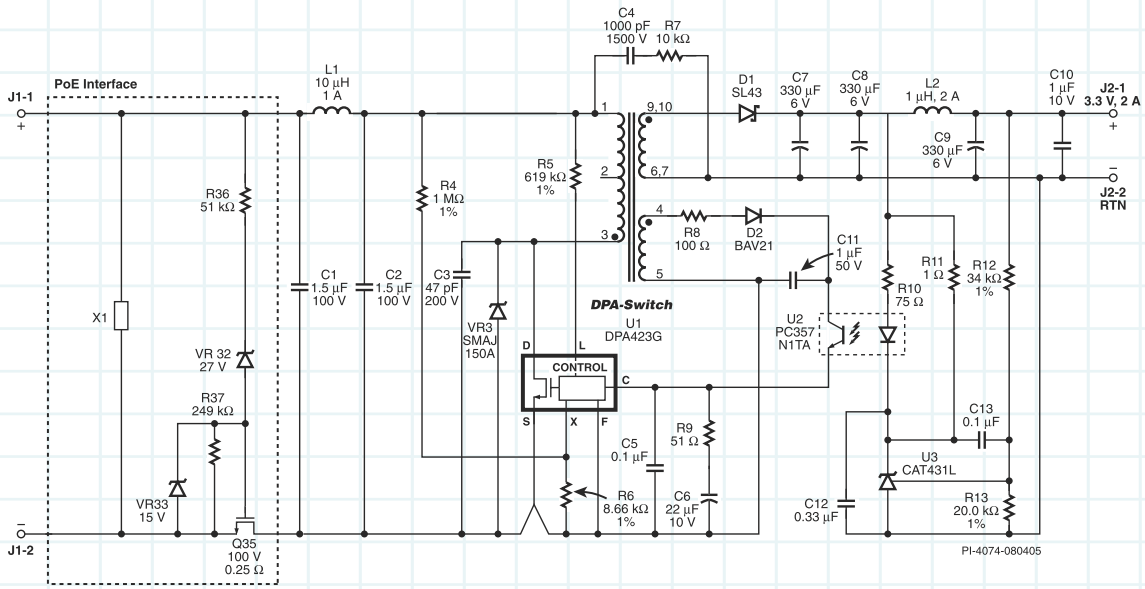
# PoE Problem to Ponder

*by Peter Vaughan*
*Manager of Product Applications*
*Power Integrations*

Test your power supply design knowledge as it pertains to Power over Ethernet by trying your hand at answering the three questions below. Check your answers at ***www.powerint.com/puzzler6*** and enter for a chance to win a new Apple iPod Mini.

The schematic below shows a typical Flyback PoE power supply built with a *DPA-Switch*® power conversion IC and a discrete PoE interface circuit for detection and Class 0 classification per IEEE 802.3af.




## Question 1: beginner

The PD (Powered Device) detection specification requires the PD to present an impedance of between 19 kΩ and 26.5 kΩ at input voltages between 2 VDC and 10 VDC. The classification stage (Class 0) requires the PD to draw a current of up to 4 mA at input voltages of between 14.5 VDC and 20.5 VDC. Is it possible to implement Class 0 detection and classification features of a PD using a single **passive** component (X1)? What is this component and component value?

## Question 2 : advanced

The PoE standard requires a wide under-voltage lockout hysteresis. The maximum cable impedance from the PSE (Power Sourcing Equipment) to the PD is 20 Ω (up to 100 meters of cable). The PSE output voltage is nominally 44 VDC with a maximum continuous output current of 350 mA. At this current level, what is the voltage at the PD end of the cable? Why is the hysteresis important?

## Question 3 : expert

The PD inrush current should be less than 450 mA after 1 ms. This allows the input capacitors of the PD to charge during startup, once the PSE output voltage exceeds 30 VDC. In a particular application, the PSE is connected via a 20 Ω cable to a PD with input capacitance of 3 µF. The PD is turned on as the PSE reaches 30 V. How long will it take for the PD input current to drop below 450 mA? Does the PD meet the PoE requirements? Does the circuit above require any additional inrush limiting components to meet the requirements?

Recalculate the same parameters with an input capacitance of 180 µF. Would any additional inrush current limit circuit be required?

*The answers to these questions can be found at* ***www.powerint.com/puzzler6****. Check out how well you did and enter to win an Apple iPod Mini!*

Finally, note that the SPEC routines are relatively immune to brief interruptions from other contending system tasks, such as mouse movement, both because they run each function multiple times and use the median result, and because each iteration takes a long time to complete. In worst-case configurations, with caches and second CPUs disabled and running nonoptimized code, a *single* SPEC benchmark iteration ran for *several days*. In contrast, each Xbench cycle takes only a minute or so to complete and comprises numerous tests, increasing the possibility that an interruption might adversely affect one or several of them. **Table 3** at www.edn.com/050915cs offers potential evidence of this corruption. One way to alleviate the situation would be to run each test multiple times to filter out the divergent data.

## THE RESULTS

Looking first at the SPEC data, you'll notice a consistent, significant performance improvement when L2 cache was enabled and a similar dramatic improvement when running O3 code versus unoptimized O0 routines. The only PowerPC 74xx-based platform on which we ran the G4-optimized SPEC routines was the Mac Mini, and it resulted in an unexpected performance *decrease* compared with O3 code. The lack of a speed boost isn't surprising; a fundamental difference between G3 and G4 PowerPC CPUs lies in the G4's AltiVec, which Apple and IBM also refer to as Velocity Engine and VMX, respectively, SIMD (single-instruction multiple-data) instruction-set support. GCC will tap into this instruction set only if it finds explicit array data-type definitions in the C source code. But the root cause of the performance decrease with supposedly G4-optimized code is unclear.

Under SPEC, the Mac Mini and PowerBook numbers are nearly identical; the slight discrepancy is likely due to random run-to-run variance, and a repeat of the experiment might even produce the opposite results. Both systems' CPUs handily beat the PowerPC 7450 in the G4 Power Mac; the G4 Power Mac's L3 cache is insufficient to counterbalance its lower core and FSB speeds and its slower cache and main memory. Note, too, that enabling the second CPU in the G4 Power Mac offered little incremental benefit. Because we ran the SPEC benchmarks in their "speed" rather than "rate" mode, the various functions executed sequentially, not in parallel. Any SPEC-benchmarking-results benefit of enabling the second CPU is likely due to its ability to handle other system functions, leaving one CPU free to focus on executing SPEC code.

Similarly, the dual G5 Power Mac results improved only slightly when we enabled the second PowerPC 970FX CPU. However, the dual G5 Power Mac did much better than its G4 counterpart when executing CPU-optimized SPEC functions. Granted, there was little performance improvement with G5-tailored code, but at least there wasn't the dramatic performance decrease seen on the Mac Mini with G4-optimized routines.

Now, turn your attention to the Xbench data. One of the first things you might notice is its contrast with the SPEC case; enabling the second CPU resulted in a demonstrable improvement in many of the Xbench test results. Enabling the

## NEW POWERPC FLAVORS

**Several weeks after Apple Chief Executive Officer Steve Jobs announced the gradual conversion of his company's computer-product lines to Intel CPUs, Freescale and IBM introduced PowerPC processors that cast some doubt on the *real* motivations behind Apple's decision. Freescale's latest G4 CPUs, manufactured on 90-nm-process technology, include the single-core MPC7448, with maximum core clock speeds of 1.7 GHz and front-side-bus speeds of 200 MHz, and the code-compatible, dual-core MPC8641D. IBM's latest offerings are a low-power variant of the single-core 970FX (G5 PowerBook, anyone?) running at 1.2 to 1.6 GHz with corresponding power consumption of 13 to 16W, and the dual-core, 2.5-GHz-maximum 970MP.**

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where you'll find the detailed report files generated by SPEC (Standard Performance Evaluation Corp) and Xbench, as well as the script files we used to compile the SPEC code; and

- "What do you observe?" where you can share your comments and peruse the observations that others have posted.

L2 cache also in most cases significantly improved the scores. Whereas the SPEC tests revealed little difference between the G4 CPUs in the Mac Mini and the PowerBook, the Xbench data magnifies the discrepancy, even if you focus only on the CPU-centric scores. Presumably, the CPU and core logic in the PowerBook are fine-tuned for power savings, whereas their counterparts in the Mac Mini are tailored for speed. And you'll notice that switching from a 4200-rpm drive to a 5400-rpm drive in the Mac Mini boosted its hard-disk drive-related test scores.

Not all of the Xbench data is predictable, however. Most baffling are the graphics-related results. Focusing on the Mac Mini, the Quartz Graphics Test numbers are unsurprisingly higher in all cases with the L2 cache enabled, but the results also increase on the 4200-rpm hard-disk drive-equipped system when system memory grows beyond 128 Mbytes. You might think, as we initially did, that this situation occurs because the graphics accelerator employs system memory as its frame buffer, but an ATI spokesperson confirms that the Radeon 9200 GPU (graphics-processing unit) has a dedicated 32-Mbyte video-memory array. Perhaps the poorer results with 128 Mbytes of system memory are due to DRAM-influenced constraints elsewhere in the system. One outstanding question is why almost all of the Mac Mini Quartz Graphics numbers are *lower* when the system is equipped with a 5400-rpm hard-disk drive. The OpenGL Graphics tests with a 5400-rpm drive versus a 4200-rpm equivalent reveal a similar performance decrease, and the 5400 rpm numbers are generally irregular; in one case, the results were actually *better* with the L2 cache off!

Unfortunately, the memory tests didn't quantifiably expose the often-dramatic system-performance improvements that we perceived when we incremented system DRAM. With 128 Mbytes of memory inside, the Mac Mini was as slow as molasses, both to initially boot and to subsequently toggle between applications (especially when coupled with a 4200-rpm hard-disk drive). Switching to a 256-Mbyte DIMM noticeably improved both attributes, and a further increase to 512 Mbytes made yet another incremental step-up, albeit not as dramatic as its predecessor. The final increase, to a 1-Gbyte DIMM, resulted in no detectable improvement, although, in a heavily loaded system with many applications simultaneously running, the difference between 512 Mbytes and 1 Gbyte of DRAM might have been more noticeable. EDN

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## ACKNOWLEDGMENT


*I'm indebted to Eric Nedervold for his abundant expertise and numerous contributions to this project.*


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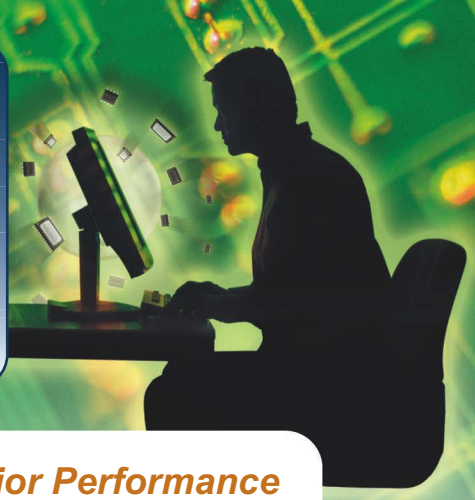

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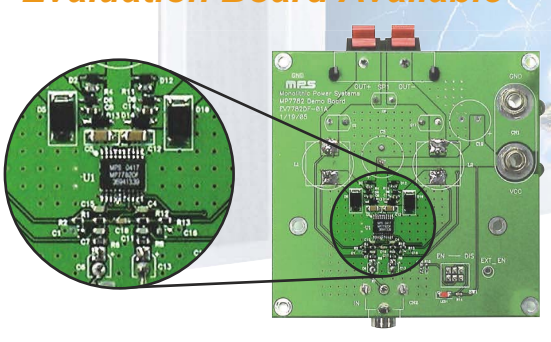

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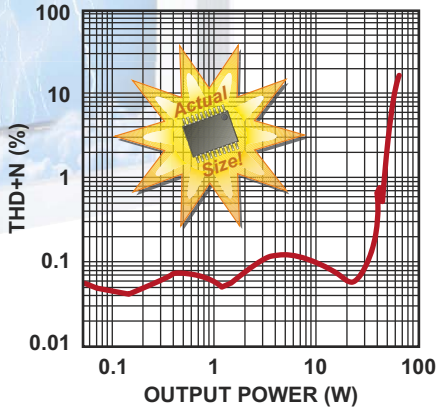



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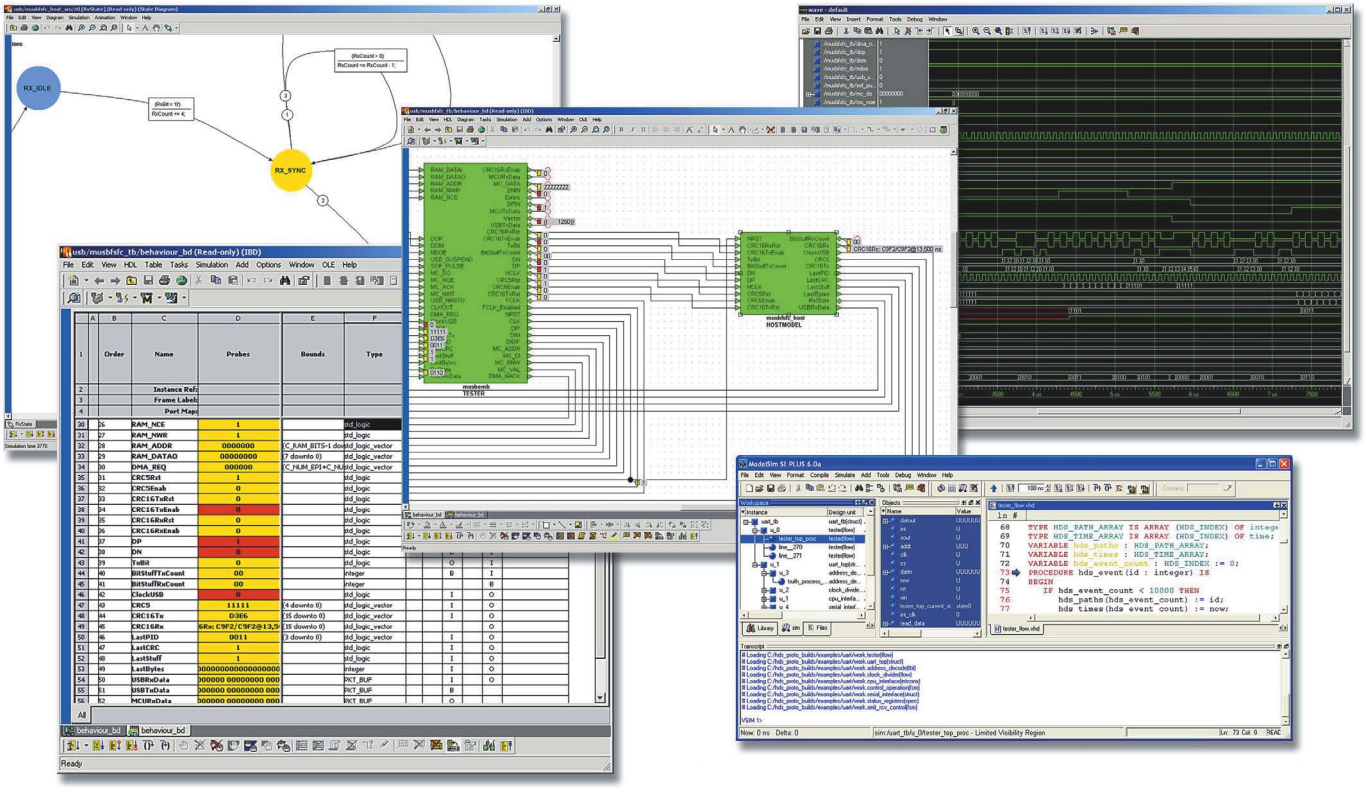

Figure 1 Mentor Graphics' FPGA Advantage is a vendor-neutral HDL-design tool for design creation, simulation, synthesis, management, and documentation.

TECH TRENDS WARREN WEBB • TECHNICAL EDITOR

# One design fits all

WITH THE LATEST FPGA TECHNOLOGY AND DROP-IN CONFIGURATION COMPONENTS, ONE BOARD DESIGN MAY SUFFICE FOR HUNDREDS OF EMBEDDED-SYSTEM APPLICATIONS.

Although board designers have for years used FPGAs (field-programmable gate arrays) to interconnect system components, the latest high-density devices are powerful enough to also replace the processors, memory, custom logic, and many peripherals of a typical embedded-system project. These new system-level or platform FPGAs allow designers to create standard hardware designs that they can tweak as new requirements emerge or that they can reconfigure for different applications. For high-performance projects with parallel computation requirements, a single platform-FPGA-board design may replace a chassis full of conventional computer boards. Yet, with the amazing capabilities of these new devices, designers must carefully analyze performance, power, and cost boundaries to determine when FPGA designs make sense.

In their simplest form, FPGAs are 2-D arrays of logic blocks with electrically programmable interconnections. Although the exact makeup differs for each FPGA vendor, logic blocks consist of transistor pairs, combinations of basic logic gates, multiplexers, or multiple-input look-up tables. Users can configure both the interconnection paths and the functions of each logic block by designating the value of built-in programming elements. Logic blocks can be a simple transistor, groups of combinational and sequential logic functions, or a complex microprocessor.

FPGA vendors have adopted several techniques for programming the interconnections and logic blocks. One of the simplest methods, the antifuse, creates a low-resistance link when you apply a high voltage across its terminals. The antifuse consumes little area but requires extra circuitry for programming. Advantages include low series resistance and low parasitic capacitance, but the main disadvantage is that an antifuse FPGA is a write-once device and therefore not re-

## AT A GLANCE

- FPGA designs allow embedded-system developers to reuse the same hardware for prototypes, revisions, and next-generation products.
- Although the per-unit price is high for FPGA devices, their parallel-processing features may reduce overall hardware requirements.
- FPGA vendors are extending performance by combining traditional logic blocks with high-bandwidth processors, memories, and custom circuitry.
- Off-the-shelf IP (intellectual-property) cores from vendors, third-party suppliers, and the open-source community simplify FPGA-design-configuration tasks.

configurable. Static-RAM cells also enable or disable pass transistors to program FPGA topology. Although at least five transistors are necessary to implement a memory cell, SRAM technology provides fast reprogrammability. SRAM-based FPGAs also require an external boot device to set the memory on power-up. Designers also use EPROM, EEPROM, and flash-memory technologies to program FPGAs with the advantages of reprogrammability and elimination of the external boot-up device. Programmable FPGA interconnections are generally slower than the permanent wiring a custom chip uses. Because the pass transistor is not a zero-resistance switch and FPGA interconnections are somewhat longer than necessary for a custom chip, the extra capacitance and resistance reduce bandwidth.

All FPGA vendors provide or offer compatibility with free or low-cost design-automation tools to capture system configurations. Designers may describe all or portions of their FPGA circuitry using an HDL (hardware-description language), such as Verilog or VHDL. Once the designer has defined the design, additional tools implement the design on a given FPGA. This process includes power and configuration optimizations; hardware partitioning, placement, and interconnection routing follow the optimizations. The output of the design-implementation phase is a bitstream file.

The design-verification phase employs a simulator to check the design's functions and maximum clock frequency. The final stage is to load the design onto the target FPGA for testing in the actual hardware environment.

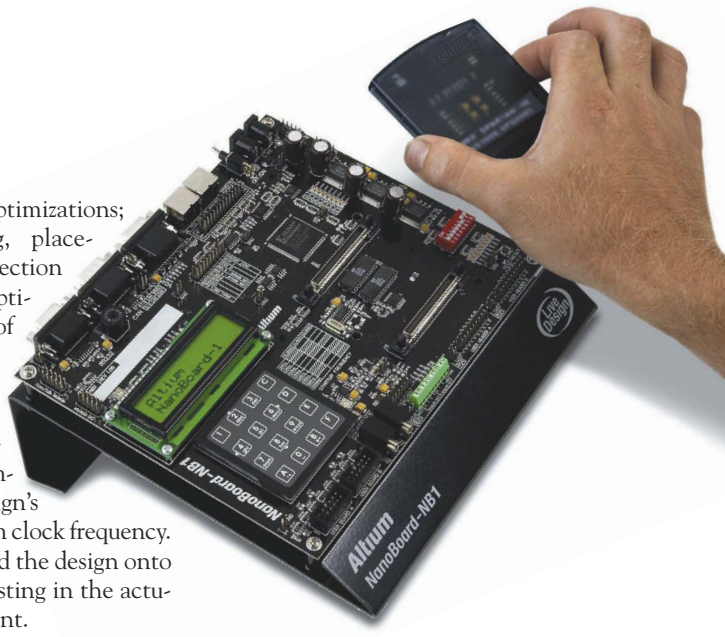


Figure 2 Altium Designer integrates board- and FPGA-level system design, embedded-software development, and pc-board layout within a single user environment.

## BRAIN CODE

The growing complexity and density of FPGA products have created a market for modular functional blocks of HDL code that designers can incorporate into their products. These functional blocks, commonly referred to as IP (intellectual-property) cores, allow manufacturers to reuse circuit elements from previous designs or simply purchase functions from an outside source. Examples of IP cores include UARTs, DSPs, Ethernet interfaces, bus interfaces, and even microcontrollers. Manufacturers physically implement hard-IP cores directly onto the silicon of an FPGA; they provide soft cores as HDL code that is portable across multiple devices.

IP cores are available from FPGA vendors; from third-party suppliers; or as freely available open-source HDL code from sources, such as www.opencores.org. Commercial IP is usually fee-based and includes documentation, verification tools, and support. According to Martin Mason, director of flash-product marketing at Actel, "We have two business models for our IP, depending on customer needs. We offer a per-use or site license that varies from as little as $200 to more than $10,000, depending on the complexity of the property. Additionally, we offer a hard-IP core for an ARM-based microcontroller that you order by special part number, and the per-unit cost of the part includes the fee for the IP."

Major FPGA vendors Xilinx and Altera, which hold more than 80% of the market share, provide extensive IP libraries for their products. Although smaller, more specialized vendors, such as Lattice, Actel, Cypress, Quicklogic, and Atmel, share the rest of the market, they also provide IP libraries. For example, Xilinx recently upgraded its popular MicroBlaze soft-IP-core processor to deliver 200-MHz performance in Virtex-4 FPGAs. The 32-bit RISC core includes an optional IEEE-754-compatible floating-point unit that allows embedded-system developers to accelerate system performance by as much as 120 times over software emulation. The MicroBlaze processor is also scalable, so designers can tune performance to match the requirements of target applications and choose greater mathematical accuracy when needed. In addition, the processor offers ready-to-use, prebuilt configuration options such as pattern-compare instructions for faster location of string, byte, or word matches. The MicroBlaze soft processor core is available as part of the $495 Xilinx EDK (embedded development kit). In addition to the MicroBlaze core, the EDK includes a set of system tools to design embedded-system applications for Xilinx FPGAs.

Although platform-FPGA capabilities are skyrocketing, designers should continue to evaluate general-purpose or custom alternatives. One of the often-cited

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drawbacks of FPGA technology is the additional power it requires compared with a general-purpose processor or custom ASIC. Most of the traditional SRAM-based FPGAs have standby currents in excess of 100 mA, which rules out most battery-operated-system applications. Likewise, because of the resistance of multiple-pass transistors and longer connection paths, FPGA-based products are also somewhat slower than conventional designs. Without taking the development time of other approaches into account, the cost of FPGA technology is substantially higher. For example, devices in Altera's latest FPGA family cost $190 to $9350, depending on the number of gates and I/O pins.

## SECURE DESIGNS

Design security is another concern for FPGA developers. In some cases, especially for SRAM designs that store configuration information and transfer it to the FPGA on power-up, IP information is vulnerable. Designers may spend months developing proprietary algorithms and configurations only to reveal the design to competitors or copycats with the first production unit. To combat IP loss, FPGA vendors use nonvolatile programming techniques along with embedded serial numbers to trace counterfeit products. Actel's Mason boasts, "We have a sophisticated security mechanism to protect internal IP. We have many customers that come to Actel for custom-marked devices, load their custom IP, and sell them as their own parts. We have no problem with that business model."

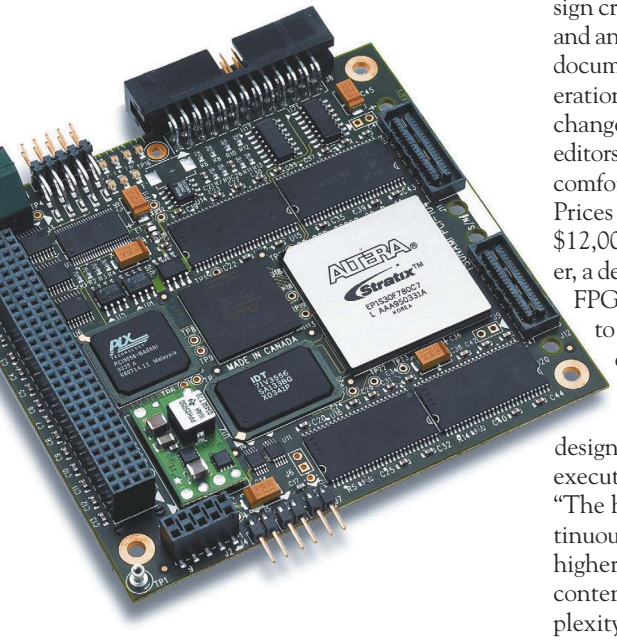


Figure 4 The Tsunami PC104 platform from SBS Technologies gives users an Altera Stratix FPGA on a 32-bit, 33-MHz PCI interface for custom processing.

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One of the most formidable obstacles to adopting FPGA technology is the steep learning curve associated with development tools. Mentor Graphics tackles this problem by offering the vendor-neutral FPGA Advantage integrated HDL-design environment. The tool enables design creation, simulation with debugging and analysis, synthesis, management, and documentation as a smooth-flowing operation from one step to the next. Interchangeable textual, tabular, and graphics editors allow designers to select their most comfortable environment (**Figure 1**). Prices for FPGA Advantage start at $12,000. Mentor also offers I/O Designer, a development tool that integrates the FPGA- and pc-board-design processes to minimize the number of signal layers and maximize signal data rates.

Altium is another tool vendor combining FPGA- and pc-board design. Nick Martin, founder and chief executive officer of Altium, explains: "The history of electronics charts a continuous movement toward designing at higher levels of abstraction to efficiently contend with increasing levels of complexity. Microprocessors and digital-design paradigms allowed portions of the design problem to move into a highly fluid and easily updatable realm: software. Today, the availability at relatively low cost of high-capacity, high-performance programmable devices, such as FPGAs, is again shifting the balance and allowing previously fixed design elements, such as the processor and its peripheral components and logic blocks, to move into a 'soft' domain." Altium Designer provides a single unified application that claims to have all the technologies and capabilities necessary for complete electronic-product development. Altium Designer integrates board- and FPGA-level system design; embedded-software development for FPGA-based processors; and pc-board layout, editing, and manufacturing within a single design environment (**Figure 2**). Unlike with HDL-design tools, electronics engineers and board-level designers can use Altium Designer without the help of dedicated HDL experts or specialized FPGA designers. The full-licensing option, which gives access to all Altium Designer capabilities, costs $11,995.

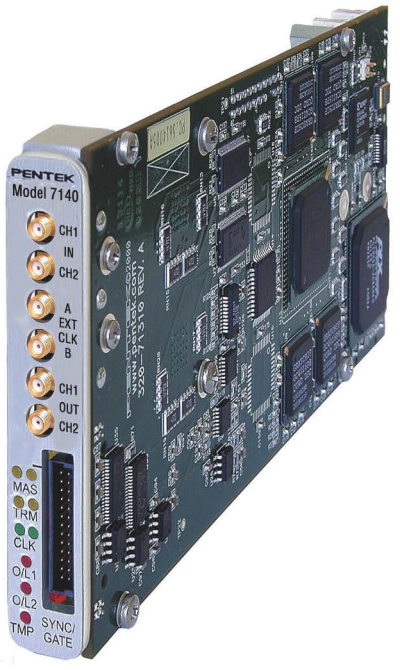


Figure 3 The Model 7140 PMC module from Pentek combines digital-radio transceivers with a Virtex II-Pro FPGA with room for user-defined DSP functions.

## PIMP MY BOARD

Embedded-board vendors have also adopted FPGA technology to offer customers off-the-shelf, reconfigurable designs. Pentek Vice President Roger Hosking comments, for example, "We have designed FPGAs into our boards for

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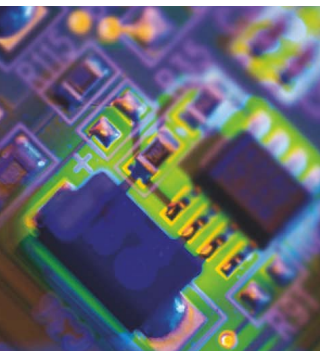

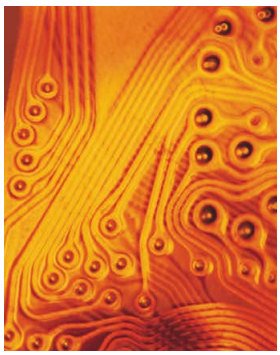

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years but only recently have we offered customers the option of reconfiguring those circuits. We use only 5 to 10% of an FPGA for standard board operations, such as signal routing, and the remaining resources are available. Now, customers can incorporate sophisticated algorithms, such as fast Fourier transforms, filters, demodulators, and digital receivers. We also offer IP-core libraries primarily for software radios. We are working on a high-density channelizer, which provides 256 narrowband digital receivers in a single FPGA. An equivalent circuit using today's four-channel ASIC downconverter would require 64 discrete packages—a huge difference in cost, space, and power. An FPGA delivers high density, but if you don't need it, use an ASIC or a general-purpose DSP."

Pentek recently introduced an FPGA-based software-radio transceiver module suitable for connection to the IF or RF ports of a communication system. The Model 7140 PMC module combines both transmitting and receiving capabilities with a high-performance Virtex II-Pro FPGA and supports the emerging VITA (VMEbus International Trade Association) 42 XMC standard with optional switched-fabric interfaces for high-speed I/O (**Figure 3**). In addition to acting as a simple transceiver, the module can perform user-defined DSP functions on the baseband signals. Such functions include demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between reception and transmission. Pentek's GateFlow FPGA Design kit provides designers with all VHDL source code and device configuration for the basic factory-installed functions to facilitate the addition of custom algorithms. Prices for the Model 7140 PMC module start at $6995.

Aimed at leveraging FPGA processing into small embedded systems, the Tsunami PC104 platform from SBS Technologies is suitable for mobile cart-based systems, machine-sensor applications, and control-I/O applications (**Figure 4**). The PC/104 Plus processor includes an Altera Stratix FPGA on a 32-bit, 33-MHz PCI interface, with enough memory and high-bandwidth datapaths to make full use of the processing power of the Stratix chip. "FPGA-based processing power comes from ASIC-like efficiency of software reprogrammable logic and the ability to parallel-process multiple streams of data," says Ron Strauss, vice president of SBS Canada. "If your embedded application requires the resources of multiple CPUs or DSPs to process the required data rate and algorithm complexity, you should instead be considering an FPGA-computing approach." The Tsunami PC104 Plus costs $4500 as a stand-alone board or $6000 with the Wave FPGA software-development-tool kit.

With today's short product life cycles, embedded-system designers need ways to create multiple system configurations with minimum custom hardware. FPGA-based products offer designers that flexibility. The reduced risk, shorter design cycles, and minimized nonrecurring-engineering charges of FPGA projects offer many advantages over ASIC-based designs. However, the added recurring cost and power required for FPGA designs limit their application to high-performance, multichannel projects. EDN

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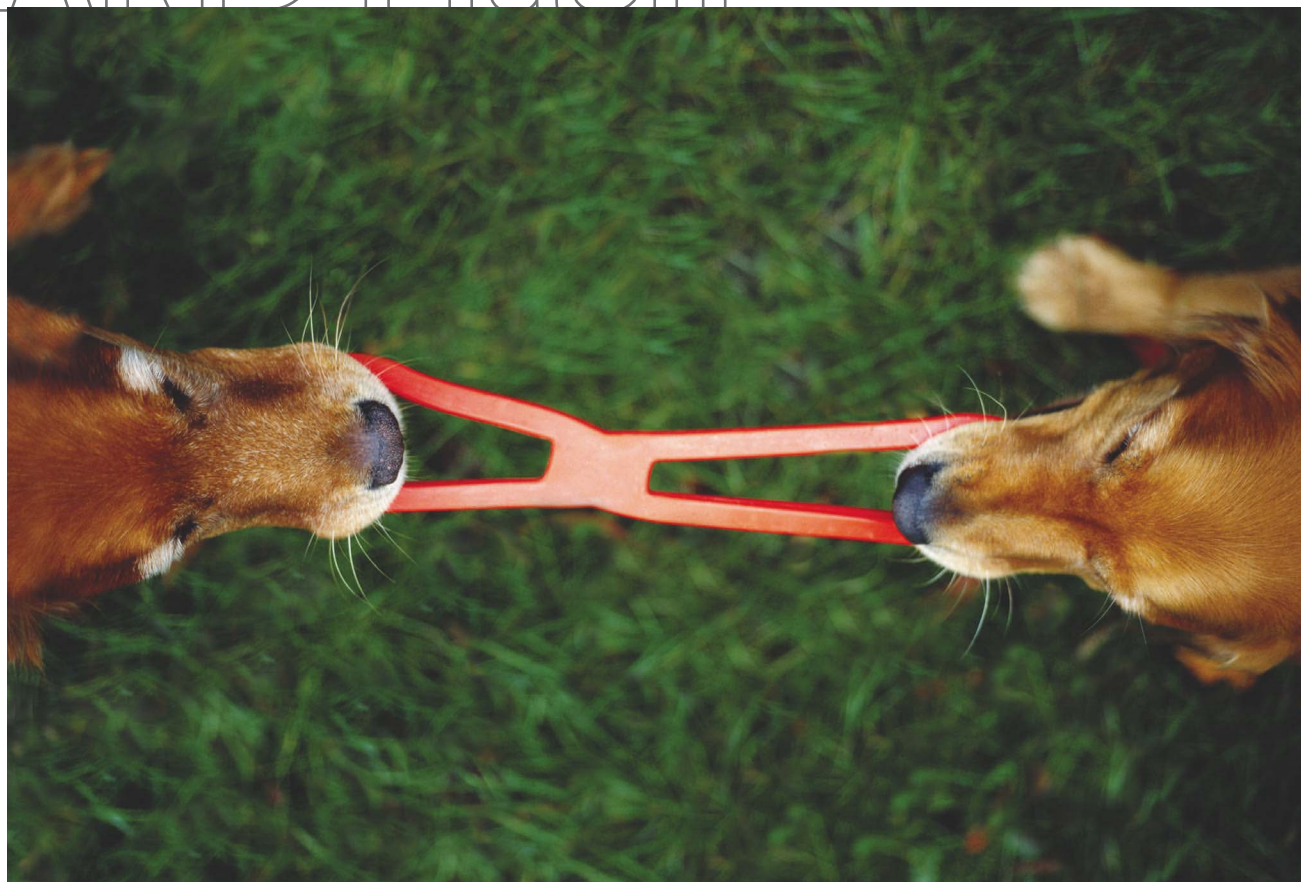

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# Meet Different Needs with NAND and NOR

By ***Richard A. Quinnell***

**FOR THE LAST FEW YEARS THE MEDIA** has debated which Flash memory technology, NAND or NOR, will emerge as the market winner. This discussion implies that the different Flash technologies are essentially interchangeable in applications, making the two direct competitors for design wins. The reality is, the two technologies address different needs.

Understanding the differences between the technologies begins with their names. The original approach to Flash memory followed the structure of other semiconductor memories, which achieve random access by connecting the memory transistors to the bit lines in parallel. Each transistor has a word line and a bit line connection. In this arrangement, if the word line turns on any memory transistor, the transistor connects drain to source and the corresponding bit line goes low. The logic function is similar to that of a "wired NOR", hence the name NOR for this arrangement.

In 1987, Toshiba proposed the NAND Flash, and its cell structure is arranged as eight memory transistors in series. The transistors are normally on, connecting drain to source through the series and keeping the bit line low. If the word line turns off any memory transistor, the transistor breaks the series connection and the bit line goes high. The logic function is similar to that of a NAND gate.

**THE TWO MAIN FLASH MEMORY TECHNOLOGIES, NAND AND NOR, ARE OFTEN VIEWED AS COMPETITORS BUT EACH ADDRESSES A DIFFERENT APPLICATION REQUIREMENT.**

These two structures result in differing attributes for the memory devices. The NOR Flash offers fast read access because its memory cells have relatively low resistance. Further, it follows conventional memory architectures, so its behavior in a system mimics that of SRAM, making it easy to design in. File storage and retrieval requires only minimal software, most of which is associated with Flash's need to erase a cell before writing to it.

## NOR reads fast, writes slow

The drawback of the NOR arrangement is that writing to cells must be done individually. Writing can take many microseconds each time it is performed. As a result, writing blocks of data to a NOR Flash takes a relatively long time because you cannot program a large number of bits simultaneously.

The NOR Flash also has the disadvantage that its memory cell is larger than that of the NAND Flash. Because each transistor has its own connection to the bit line, the cell requires more metal-layer contacts, making the transistors occupy more die area than in NAND cells, which connect in series in silicon. Because metal-layer connections are the limiting factor in scaling, the NOR Flash always lags NAND Flash in achievable bit density.

The NAND Flash structure allows a page of data to be programmed simultaneously. A page size is typically 2,112 Bytes or 16,896 bits. This greatly speeds write times. On the other hand, the higher resistance of a series connection, compared to the parallel connection used in NOR Flash, means that the NAND bit lines are relatively slow to change state, limiting read access speeds. (See Figure 1.)

But NAND Flash does not offer a conventional memory interface. Controlling a NAND Flash is similar to controlling an I/O device in that device control is achieved by writing to the NAND Flash's internal registers. A command sequence is required in order to perform a read, program, or erase operation. An advantage of this indirect interface is that it enables migration to higher chip densities with no change in pinout.

## NAND writes fast, reads slower

Block access also makes NAND Flash unsuitable for truly random access use, such as execution in place (XIP) of program code. If NAND Flash is used for code storage, the system needs to copy the code to RAM in order to execute the code. NOR Flash allows XIP.

A major advantage of NAND Flash, beyond erase and write speed improvements, is that the NAND Flash cell structure uses less die area per bit, This allows a higher bit density for a given

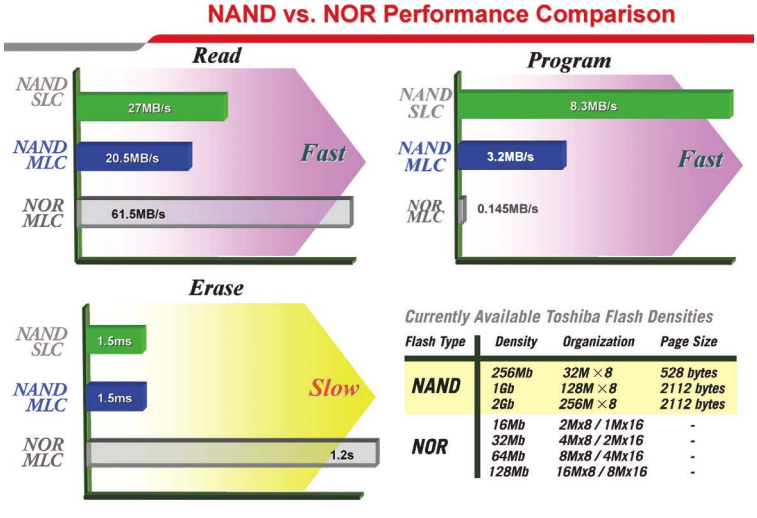



***Figure 1.*** *NAND and NOR Flash architectures have different performance characteristics, with NOR having the edge in read speed while NAND offers faster write and erase.*

SOURCE: TOSHIBA

fabrication process and a lower cost per bit for NAND Flash as compared to NOR Flash.

These relative advantages and limitations make NAND and NOR Flash architectures suited to different applications. NOR Flash performs better than NAND Flash in code storage applications, where read speed is the most critical parameter. Further, NOR's ability to support XIP means that no additional memory needs to be involved in order to run the stored code. Code storage typically does not require the highest density memory, so the cell size restrictions are not significant in this application.

NAND Flash performs best in data storage applications. It was originally developed to function like and replace magnetic storage, such as disk drives. In data storage, write speed is the most important performance parameter, so the speed advantage of NAND Flash makes it the best architecture for data storage. Read speed is a secondary concern in data storage, although it should be at least as fast as the write speed. The read speed of any Flash memory is greater than its write speed, however, so the performance of NAND Flash meets the read requirements of data storage, as well.

Capacity, however, is a critical concern in data storage. Data storage can require thousands of times the capacity needed for code storage. As a result, both total capacity and cost per bit become important for data storage needs. The smaller cell size of NAND Flash further points to this architecture as the best choice for data storage.

## Flash types fit different applications

The differing application strengths for Flash architectures thus allows for both NOR and NAND to co-exist in the market, and even in the same design. In a cell phone, for example, NOR Flash can serve as code storage where the memory's XIP capability eliminates any need for shadow RAM. NAND Flash can serve as data storage for large memory files such as photos and video.

The situation may eventually change, however. NOR Flash is increasing in density and in write speed with each process generation. Although NOR will never catch up to NAND, these density increases allow NOR to stay ahead of increasing storage requirements in smaller applications. For those applications, NOR's design simplicity gives it a cost advantage over NAND Flash.

NAND Flash, on the other hand, continues to lead in cost, density, and write performance. The existence of a powerful NAND Flash controller is making design-in easier, so for larger applications NAND Flash becomes the lower cost option.

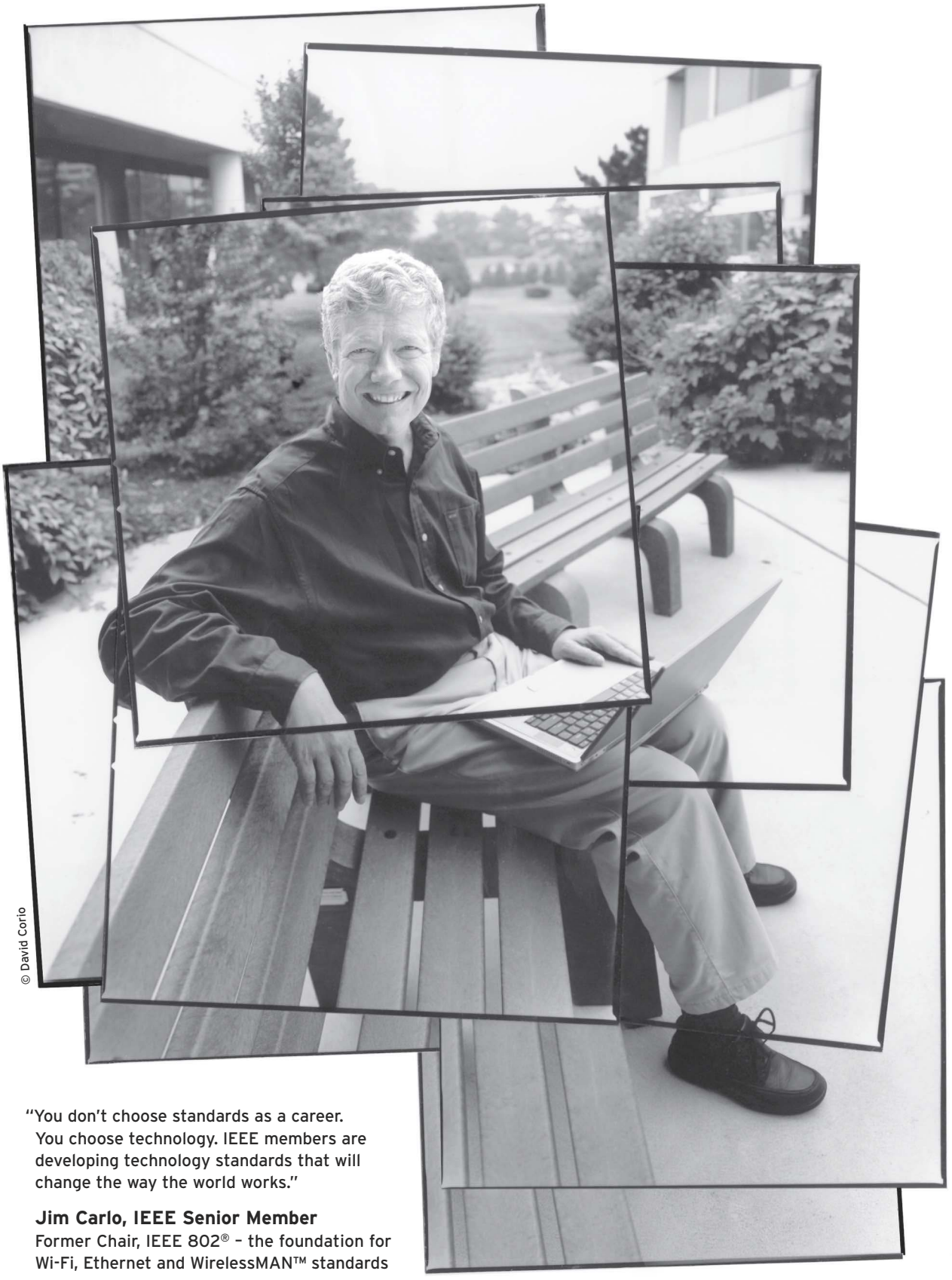
**ADDITIONAL INFO**

- *To learn more about Flash memory visit www.edn.com/NANDflashmemory*
- *For more information on Toshiba's NOR and NAND Flash go to www.toshiba.com*

The largest single market for Flash memory is the cell phone, and high-end cell phones are using ever faster processors. These processors are beginning to force use of shadow RAM for code storage regardless of the Flash in use because no Flash technology is keeping pace with high-end processor read speeds. In addition, high-end cell phones are increasing their need for data storage to provide feature convenience. The addition of cameras, movies, MP3 audio, gaming, and Internet access to phones requires significant amounts of low-cost storage.

These trends are affecting the sweet spot for Flash memory. The high performance applications are beginning to favor NAND Flash for both code and data storage. NOR will still have a home in low-performance code storage, however, so both architectures will continue to co-exist in the market. All that remains uncertain is when the high-volume markets will switch to NAND alone. ■

**ABOUT THE EDITOR:** *Richard A. Quinnell was an embedded systems designer for 15 years before turning to technology journalism. He was a staff writer for EDN for 10 years and is now a contributing editor and freelance writer for a number of high-tech publications.*



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IEEE

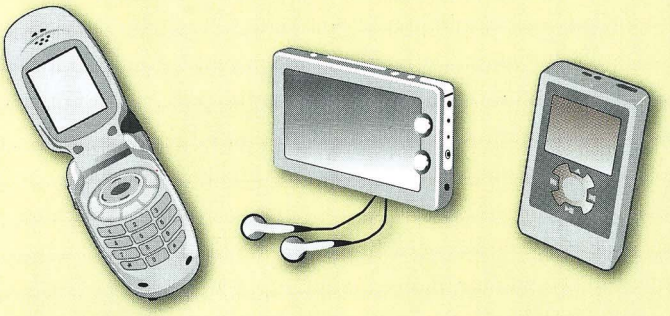
# World's Smallest Video Driver

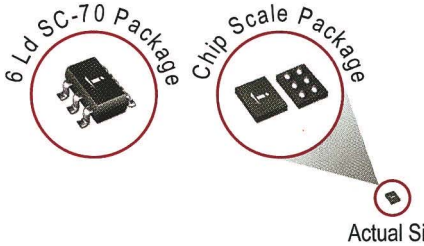
**ISL59110 and ISL59111 8MHz rail-to-rail composite video drivers meet the high demands of micropower and bandwidth in battery-operated applications**

Space Efficient Package

Available in Pb-Free Package

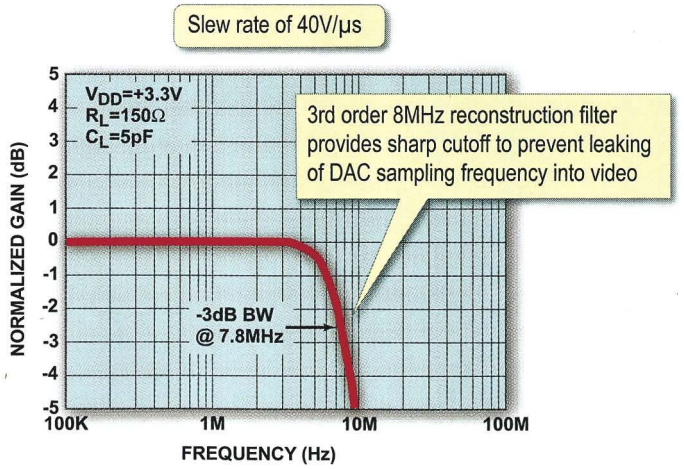
Ideal for driving composite video out in portable media players



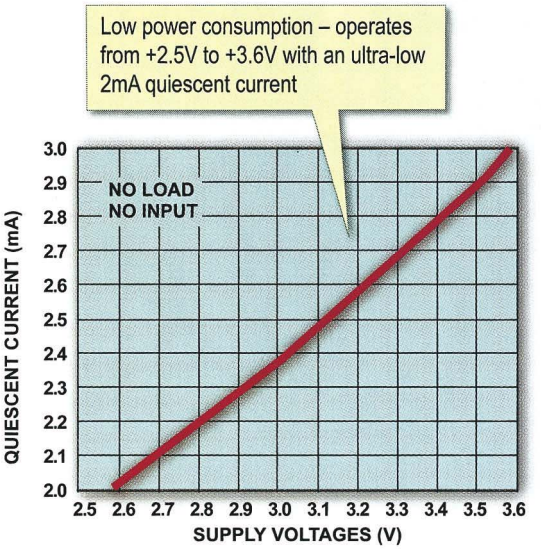



**Key Features:**

- Available in SC-70 package or smallest 1mm x 1.5mm chip scale package
- Low supply current of 2mA and power-down current of less than 3µA saves battery life




GAIN vs FREQUENCY -3dB POINT

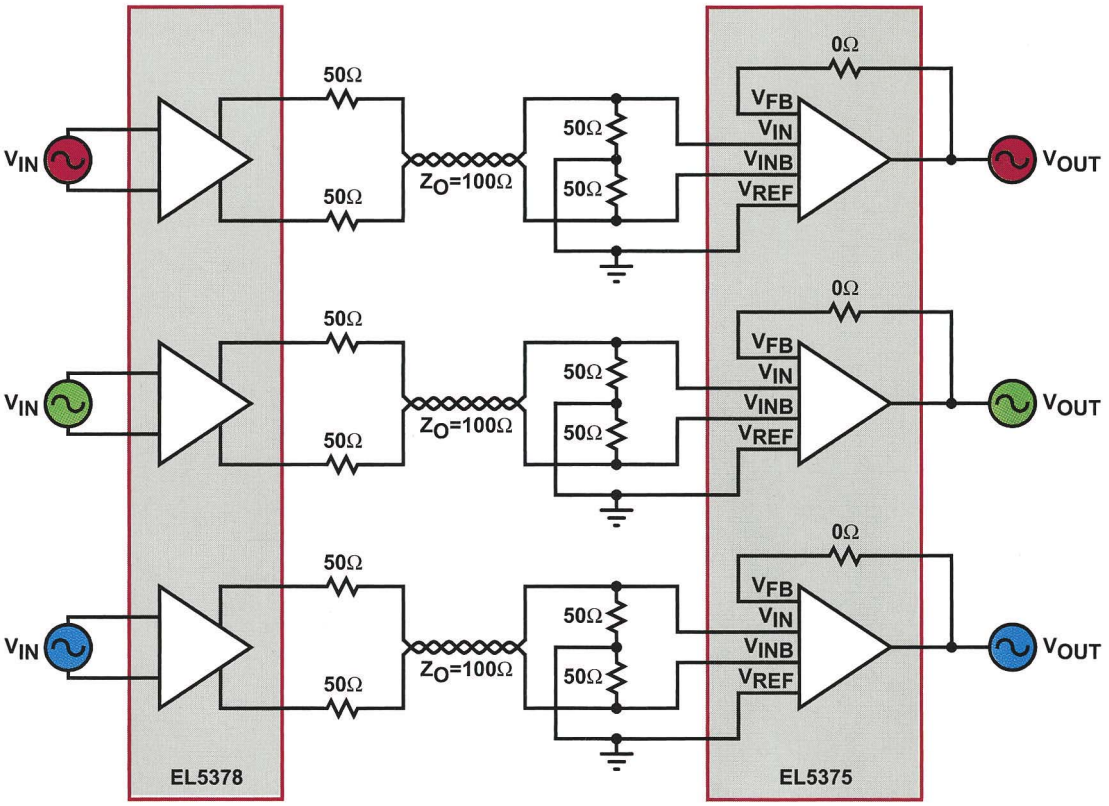



SUPPLY CURRENT vs SUPPLY VOLTAGE

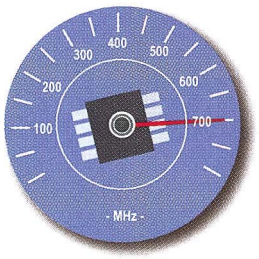
# World's Fastest Triple Differential Driver

## EL5378 (EL5178) 700MHz Differential Twisted-Pair Drivers

*Fixed gain version shown*
*Programmable gain version available*




*Receiver feedback resistors are external*




**700MHz**

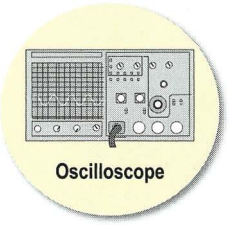
**Key Features:**

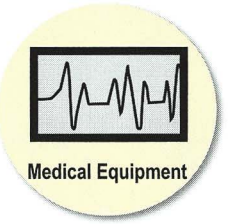
- Fully differential inputs, outputs, and feedback
- Differential input range ±2.3V
- 700MHz 3dB bandwidth
- 1000V/µs slew rate
- Low distortion at 5MHz
- Single 5V or dual ±5V supplies
- 60mA maximum output current
- Low power - 12.5mA per channel

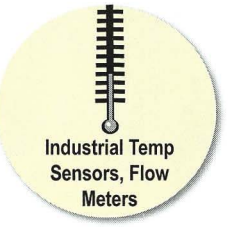
# World's First 30V, >200MHz Quad Voltage Feedback Amplifier

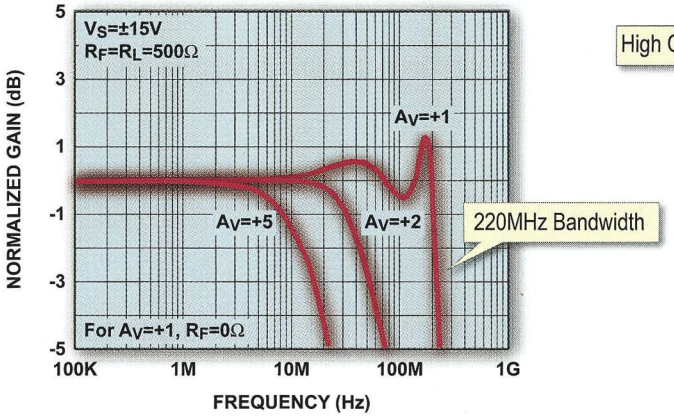
Available in Pb-Free Package

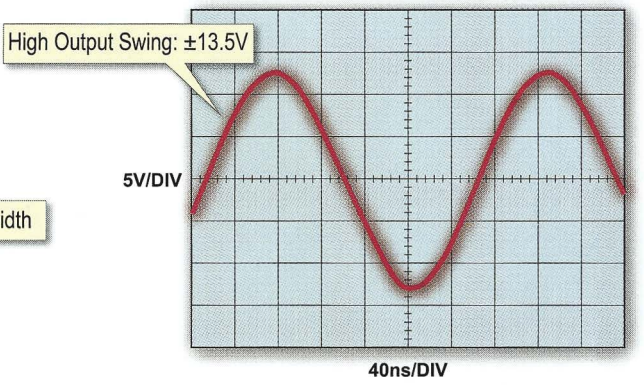
**ISL55002 and ISL55004 high voltage unity-gain stable op amps**

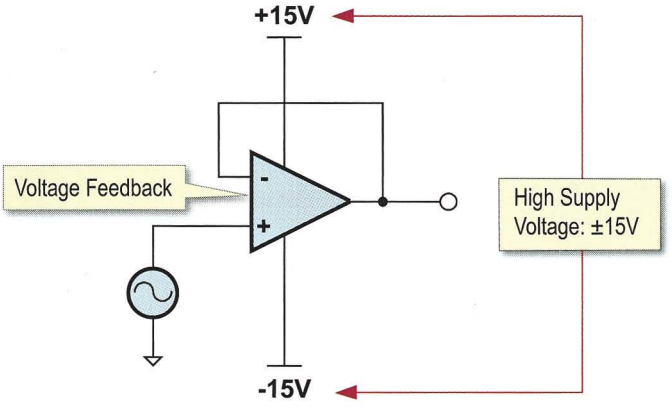


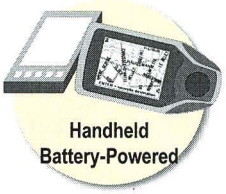



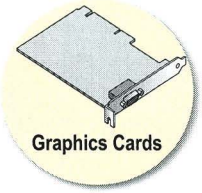



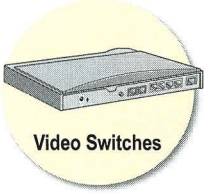

**Key Features:**

- 220MHz -3dB bandwidth
- Unity-gain stable
- Wide output swing
- Low supply current: 9mA @ $V_S$ = ±15V
- Wide supply range: ±2.5V to ±15V (dual supply) and 5V to 30V (single supply)
- High slew rate: 300V/µs
- Fast settling: 75ns to 0.1% for a 10V step

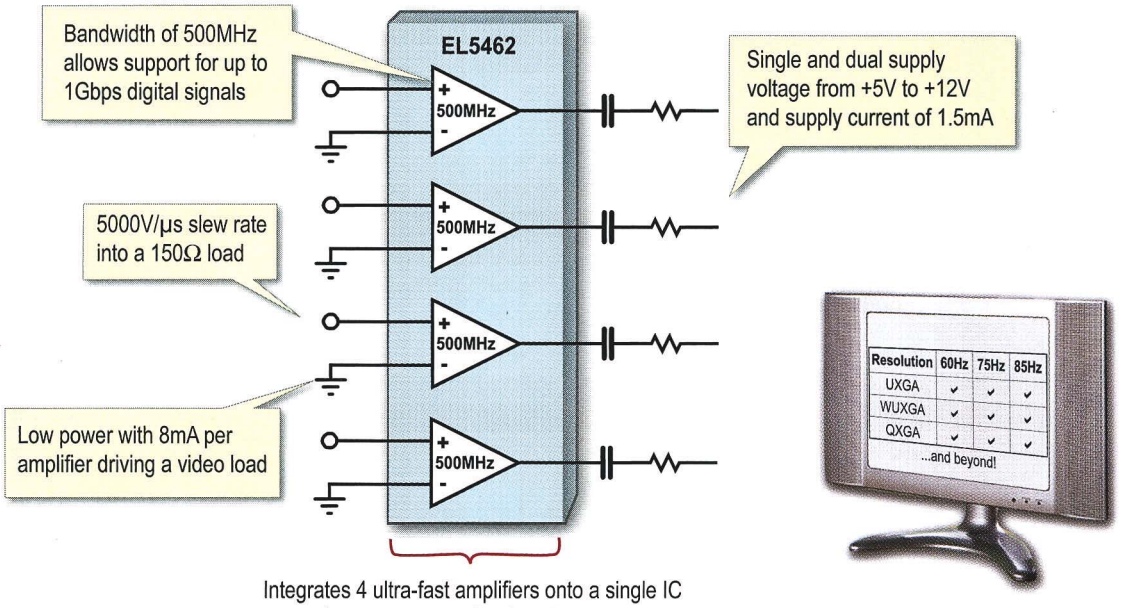
# Low Power Quad Current Feedback Amplifier Drives Resolutions Beyond QXGA


Available in Pb-Free Package



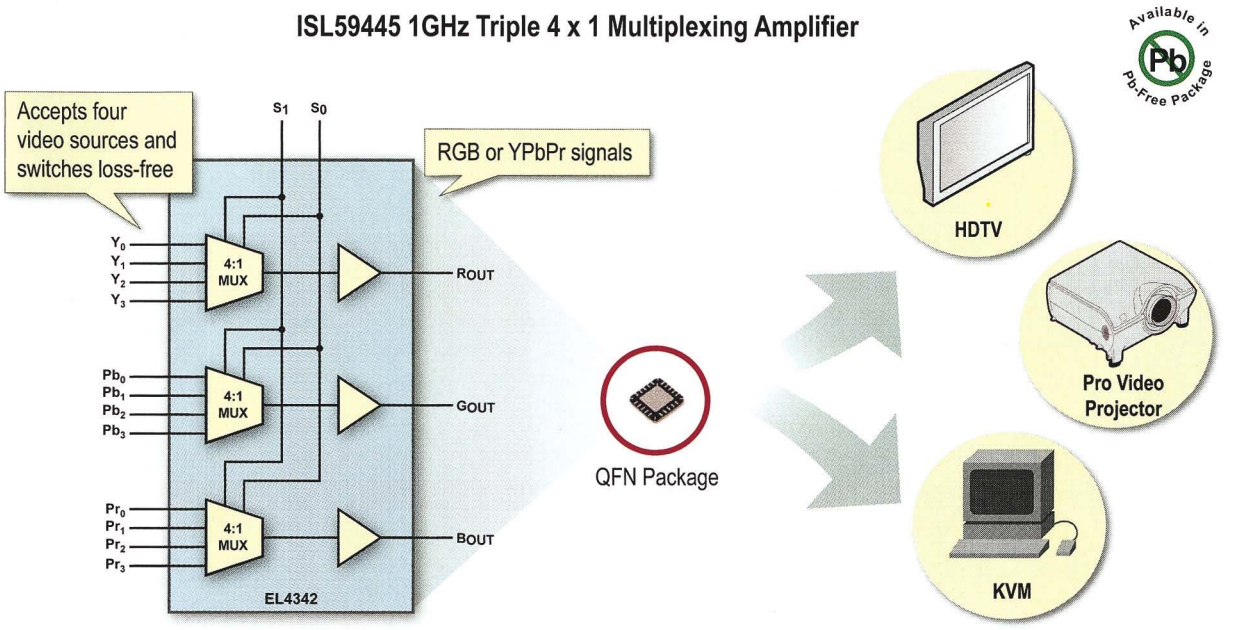

Integrates 4 ultra-fast amplifiers onto a single IC for space-constrained applications

**Video Amplifiers - High Speed (>50MHz)**

| Device | # of Amps | BW @ -3dB (MHz) | Slew Rate (V/µs) | $V_S$ (min) (V) | $V_S$ (max) (V) | $V_N$ (nV/√Hz) | Gain $A_V$ (min) (V) | $I_S$ (per amp) (mA) | $I_{OUT}$ (mA) | $V_{OUT}$ (V) | $V_{OS}$ (max) (mV) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| EL5160, EL5161 | 1 | 200 | 1700 | ±2.5 | ±5.5 | 4 | 1 | 0.75 | 70 | ±3.4 | 5 |
| EL5260, EL5261 | 2 | 200 | 2000 | ±2.25 | ±6.6 | 4 | 1 | 0.75 | 70 | ±3.4 | 5 |
| EL5360 | 3 | 200 | 1700 | ±2.25 | ±6.3 | 4 | 1 | 0.75 | 70 | ±3.4 | 5 |
| EL5162, EL5163 | 1 | 500 | 4000 | ±2.5 | ±5.5 | 3 | 1 | 1.5 | 100 | ±3.6 | 5 |
| EL5262, EL5263 | 2 | 500 | 2500 | ±2.25 | ±6.6 | 3 | 1 | 1.5 | 100 | ±3.6 | 5 |
| EL5362 | 3 | 500 | 2500 | ±2.25 | ±6.3 | 3 | 1 | 1.5 | 100 | ±3.6 | 5 |
| EL5462 | 4 | 500 | 4000 | ±2.5 | ±5.5 | 3 | 1 | 1.5 | 100 | ±3.75 | 1.5 |
| EL5164, EL5165 | 1 | 600 | 4700 | ±2.5 | ±5.5 | 2.1 | 1 | 3.5 | 140 | ±3.8 | 3.5 |
| EL5364 | 3 | 600 | 4200 | ±2.25 | ±6.3 | 2 | 1 | 3.5 | 140 | ±3.8 | 5 |
| EL5191 | 1 | 1000 | 2800 | ±2.25 | ±5.5 | 3.8 | 1 | 9 | 120 | ±3.7 | 15 |
| EL5367 | 3 | 1000 | 5000 | ±2.25 | ±5.5 | 1.7 | 1 | 8.5 | 160 | ±3.8 | 5 |
| EL5166 | 1 | 1400 | 6000 | ±2.5 | ±5.5 | 1.7 | 1 | 8.5 | 160 | ±3.8 | 5 |

# 1GHz Component Video MUX

## ISL59445 1GHz Triple 4 x 1 Multiplexing Amplifier




### Key Features:

- Set to gain-of-1 (fixed)
- High-speed 3-state outputs
- Power-down mode
- ±5V operation
- 1GHz -3dB bandwidth
- QFN packaging

### Video MUXes with Integrated Op Amps

| Device | Configuration | BW @ -3dB (MHz) | SR (V/µs) | $I_S$ (V) | Gain $A_V$ (min) (V) | $I_{OUT}$ (mA) | Diff Gain (%) | Diff Phase (°) | Package |
|---|---|---|---|---|---|---|---|---|---|
| ISL59420 | 2 to 1 | 500 | 900 | 5 | 1 | 100 | 0.05 | 0.05 | 10 Ld MSOP |
| ISL59440 | 4 to 1 | 500 | 900 | 7 | 1 | 100 | 0.05 | 0.05 | 16 Ld QSOP |
| ISL59421 | 2 to 1 | 1000 | 1500 | 10 | 1 | 100 | 0.05 | 0.05 | 10 Ld MSOP |
| ISL59441 | 4 to 1 | 1000 | 1500 | 14 | 1 | 100 | 0.05 | 0.05 | 16 Ld QSOP |
| EL4340 | Triple 2 to 1 | 500 | 900 | 11 | 1 | 100 | 0.05 | 0.05 | 24 Ld QSOP |
| EL4342 | Triple 4 to 1 | 500 | 900 | 16 | 1 | 100 | 0.05 | 0.05 | 32 Ld QFN |
| ISL59424 | Triple 2 to 1 | 1000 | 1500 | 22 | 1 | 100 | 0.05 | 0.05 | 24 Ld QFN |
| ISL59445 | Triple 4 to 1 | 1000 | 1500 | 32 | 1 | 100 | 0.05 | 0.05 | 32 Ld QFN |

### Switches

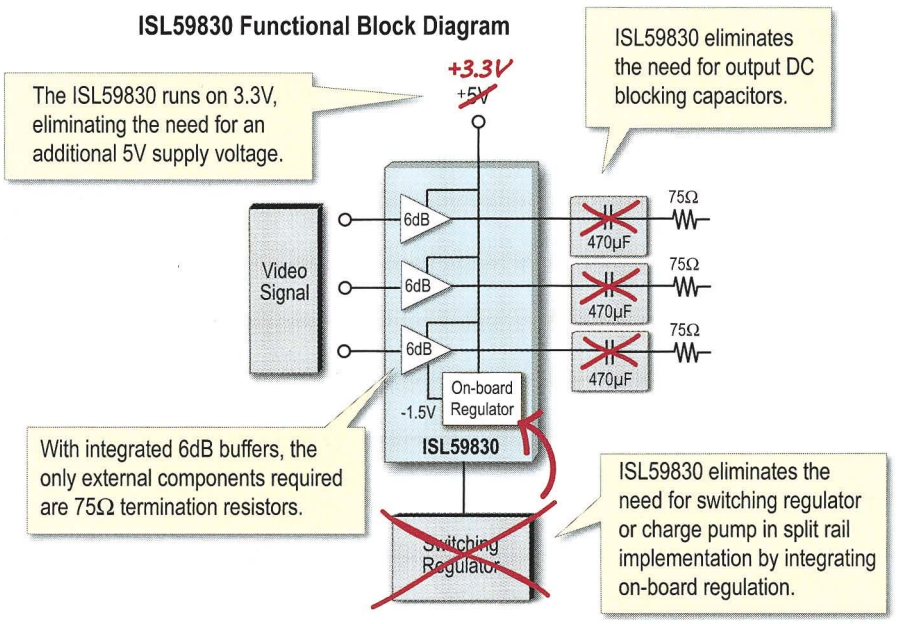
| Device | Configuration | $R_{ON}$ @ 5V (Ω) | $T_{(ON)}$ (ns) | $T_{(OFF)}$ (ns) | BW @ -3dB (MHz) | Off Cap (pF) | On Cap (pF) | $I_S$ (µA) | $V_S$ (V) | Package |
|---|---|---|---|---|---|---|---|---|---|---|
| ISL43110 | Single NO | 11 | 37 | 21 | 220 | 15 | 40 | 0.05 | +2.4 to +12 | 5 Ld SOT-23, 8 Ld SOIC |
| ISL84514 | Single NO | 13 | 47 | 28 | 220 | 14 | 30 | 2 (Max) | +2.4 to +12 | 5 Ld SOT, 8 Ld SOIC |
| ISL43144 | Quad NO | 18 | 52 | 40 | 330 | 10 | 34 | 0.01 | +2 to +12, ±2 to ±6 | 16 Ld QFN, 16 Ld TSSOP |
| ISL8392 | Quad NO | 20 | 60 | 30 | 330 | 12 | 34 | 0.01 | +2 to +12, ±2 to ±6 | 16 Ld SOIC |
| ISL43210 | Single 2x1 | 19 | 25 | 17 | 500 | 8 | 28 | 0.05 | +2.7 to +12 | 6 Ld SOT-23 |
| ISL43231 | Triple 2x1 | 81 | 32 | 18 | 250 | 3 | 14 | 0.1 | +2 to +12, ±2 to ±6 | 20 Ld QFN |
| ISL84053 | Triple 2x1 | 125 | 50 | 40 | 250 | 3 | 14 | 0.1 | +2 to +12, ±2 to ±6 | 16 Ld QSOP, 16 Ld SOIC |
| ISL43240 | Quad 2x1 | 30 | 52 | 40 | 330 | 10 | 30 | 0.01 | +2 to +12, ±2 to ±6 | 20 Ld QFN, 20 Ld SSOP |
| ISL8394 | Quad 2x1 | 25 | 50 | 30 | 330 | 12 | 39 | 0.01 | +2 to +12, ±2 to ±6 | 20 Ld SOIC |
| ISL43640 | Single 4 x1 | 115 | 25 | 24 | 350 | 4 | 20 | 0.0001 | +2 to +12 | 10 Ld MSOP, 16 Ld QFN |
| ISL43840 | Dual 4x1 | 81 | 32 | 18 | 250 | 3 | 18 | 0.1 | +2 to +12, ±2 to ±6 | 20 Ld QFN |
| ISL43841 | Dual 4x1 | 81 | 32 | 18 | 250 | 3 | 18 | 0.1 | +2 to +12, ±2 to ±6 | 20 Ld QFN |
| ISL43741 | Diff 4x1 | 81 | 32 | 18 | 280 | 3 | 18 | 0.1 | +2 to +12, ±2 to ±6 | 20 Ld QFN |
| ISL43681 | Single 8x1 | 81 | 32 | 18 | 250 | 3 | 26 | 0.1 | +2 to +12, ±2 to ±6 | 20 Ld QFN |

# Eliminate Extra Voltage Supply with Integrated Triple +3.3V Video Buffer

**The ISL59830 triple video buffer delivers DC-accurate coupling of video onto a 75Ω double-terminated line, and 300MHz of -3dB bandwidth performance.**

Available in Pb-Free Package

**ISL59830 Functional Block Diagram**



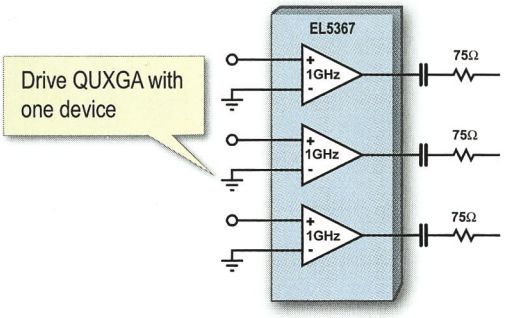

**Key Features:**

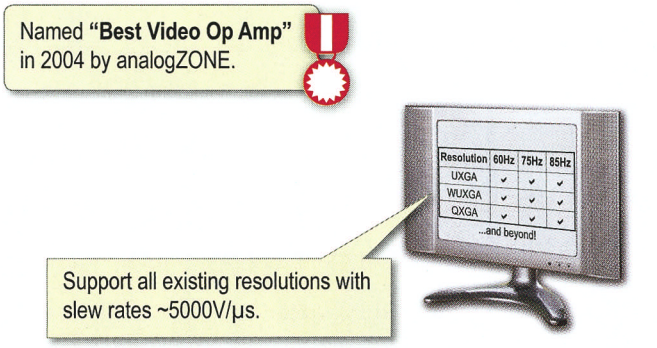
- Triple single-supply buffer
- Operates from single +3.3V supply
- Eliminates need for DC blocking capacitors
- Fixed gain of 2 output buffer
- Output 3-statable
- Enable/disable functions
- 50MHz 0.1dB bandwidth
- 300MHz -3dB bandwidth

**Video Amplifiers - Rail-to-Rail**

| Device | # of Amps | BW @ -3dB (MHz) | SR (V/µs) | $V_S$ (V) | $V_N$ (nV√Hz) | Rail-to-Rail | Gain $A_V$ (min) (V) | $I_S$ (mA) | $I_{BIAS}$ (mA) | $I_{OUT}$ (mA) | $V_{OUT}$ (V) | $V_{OS}$ (max)(mV) | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EL8100 | 1 | 200 | 200 | 3.3 to 5 | 20 | Out | 1 | 2 | 1.5 | 80 | 0.1 to 4.9 | 6 | 6 Ld SOT-23, 8 Ld SOIC, 8 Ld SOT-23 |
| EL8101 | 1 | 200 | 200 | 3.3 to 5 | 20 | Out | 1 | 2 | 1.5 | 80 | 0.1 to 4.9 | 6 | 5 Ld SOT-23 |
| EL8102 | 1 | 500 | 600 | 3.3 to 5 | 12 | Out | 1 | 5.6 | 6 | 150 | 0.1 to 4.9 | 8 | 6 Ld SOT-23, 8 Ld SOIC |
| EL8103 | 1 | 500 | 600 | 3.3 to 5 | 12 | Out | 1 | 5.6 | 6 | 150 | 0.1 to 4.9 | 8 | 5 Ld SOT-23 |
| EL8200 | 2 | 200 | 200 | 3.3 to 5 | 20 | Out | 1 | 2 | 1.5 | 65 | 0.1 to 4.9 | 6 | 10 Ld MSOP |
| EL8201 | 2 | 200 | 200 | 3.3 to 5 | 20 | Out | 1 | 2 | 1.5 | 80 | 0.1 to 4.9 | 6 | 8 Ld SOIC |
| EL8202 | 2 | 500 | 600 | 3.3 to 5 | 12 | Out | 1 | 5.6 | 6 | 65 | 0.1 to 4.9 | 8 | 10 Ld MSOP |
| EL8203 | 2 | 500 | 600 | 3.3 to 5 | 12 | Out | 1 | 5.6 | 6 | 150 | 0.1 to 4.9 | 8 | 8 Ld MSOP, 8 Ld SOIC |
| EL8300 | 3 | 200 | 200 | 3.3 to 5 | 20 | Out | 1 | 2 | 1.5 | 80 | 0.1 to 4.9 | 6 | 16 Ld QSOP, 16 Ld SOIC |
| EL8302 | 3 | 500 | 600 | 3.3 to 5 | 15 | Out | 1 | 6 | 6 | 150 | 0.1 to 4.9 | 8 | 16 Ld QSOP, 16 Ld SOIC |
| EL8401 | 4 | 200 | 200 | 3.3 to 5 | 20 | Out | 1 | 2 | 1.5 | 80 | 0.1 to 4.9 | 8 | 14 Ld SOIC, 16 Ld QSOP |
| EL8403 | 4 | 500 | 600 | 3.3 to 5 | 12 | Out | 1 | 5.6 | 6 | 65 | 0.1 to 4.9 | 8 | 14 Ld SOIC, 16 Ld QSOP |
| ISL59830 | 3 | 200 | 500 | 3.0 to 3.6 | 20 | Y | 2 | 50 | N/A | 50/-18 | -1.8 to 3.3 | 25 | 16 Ld QSOP |

# World's Fastest Triple Current Feedback Amp




**Video Amplifiers - High Speed (>50MHz)**

| | Device | # of Amps | BW @ -3dB (MHz) | Slew Rate (V/µs) | $V_S$ (min) (V) | $V_S$ (max) (V) | $V_N$ (nV/√Hz) | Gain $A_V$ (min) (V) | $I_S$ (per amp) (mA) | $I_{OUT}$ (mA) | $V_{OUT}$ (V) | $V_{OS}$ (max) (mV) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Current Feedback | EL5160, EL5161 | 1 | 200 | 1700 | ±2.5 | ±5.5 | 4 | 1 | 0.75 | 70 | ±3.4 | 5 |
| | EL5260, EL5261 | 2 | 200 | 2000 | ±2.25 | ±6.6 | 4 | 1 | 0.75 | 70 | ±3.4 | 5 |
| | EL5360 | 3 | 200 | 1700 | ±2.25 | ±6.3 | 4 | 1 | 0.75 | 70 | ±3.4 | 5 |
| | EL5162, EL5163 | 1 | 500 | 4000 | ±2.5 | ±5.5 | 3 | 1 | 1.5 | 100 | ±3.6 | 5 |
| | EL5262, EL5263 | 2 | 500 | 2500 | ±2.25 | ±6.6 | 3 | 1 | 1.5 | 100 | ±3.6 | 5 |
| | EL5362 | 3 | 500 | 2500 | ±2.25 | ±6.3 | 3 | 1 | 1.5 | 100 | ±3.6 | 5 |
| | EL5462 | 4 | 500 | 4000 | ±2.5 | ±5.5 | 3 | 1 | 1.5 | 100 | ±3.75 | 1.5 |
| | EL5164, EL5165 | 1 | 600 | 4700 | ±2.5 | ±5.5 | 2.1 | 1 | 3.5 | 140 | ±3.8 | 3.5 |
| | EL5364 | 3 | 600 | 4200 | ±2.25 | ±6.3 | 2 | 1 | 3.5 | 140 | ±3.8 | 5 |
| | EL5191 | 1 | 1000 | 2800 | ±2.25 | ±5.5 | 3.8 | 1 | 9 | 120 | ±3.7 | 15 |
| | EL5367 | 3 | 1000 | 5000 | ±2.25 | ±5.5 | 1.7 | 1 | 8.5 | 160 | ±3.8 | 5 |
| | EL5166 | 1 | 1400 | 6000 | ±2.5 | ±5.5 | 1.7 | 1 | 8.5 | 160 | ±3.8 | 5 |
| Voltage Feedback | EL5170 | 1 | 100 | 1100 | ±2.25 | ±6.0 | 28 | 2 (Fixed) | 7 | 80 | ±3.3 | 25 |
| | EL5370 | 3 | 100 | 1200 | ±2.25 | ±6.0 | 28 | 2 (Fixed) | 7 | 85 | ±3.8 | 25 |
| | EL5100, EL5101 | 1 | 200 | 2200 | ±2.25 | ±6.6 | 10 | 1 | 2.5 | 100 | ±3.4 | 4 |
| | EL5300 | 3 | 200 | 2200 | ±2.25 | ±6.6 | 10 | 1 | 2.5 | 100 | ±3.4 | 4 |
| | EL5371 | 3 | 250 | 700 | ±2.25 | ±6.0 | 26 | 1 | 7 | 70 | ±3.7 | 25 |
| | EL5372 | 3 | 250 | 800 | ±2.25 | ±6.6 | 26 | 1 | 5 | 95 | ±3.6 | 25 |
| | EL5106 | 1 | 350 | 4500 | ±2.25 | ±6.6 | 12 | ±1, 2 (Fixed) | 1.5 | 125 | ±3.6 | 10 |
| | EL5306 | 3 | 350 | 4500 | ±2.25 | ±6.6 | 12 | ±1, 2 (Fixed) | 1.5 | 125 | ±3.6 | 10 |
| | EL5102, EL5103 | 1 | 400 | 2200 | ±2.25 | ±6.6 | 6 | 1 | 5.2 | 150 | ±3.7 | 5 |
| | EL5202, EL5203 | 2 | 400 | 2200 | ±2.5 | ±6.6 | 6 | 1 | 5.2 | 150 | ±3.9 | 5 |
| | EL5302 | 3 | 400 | 2200 | ±2.25 | ±6.6 | 6 | 1 | 5.2 | 150 | ±3.7 | 5 |
| | EL5173 | 1 | 450 | 900 | ±2.25 | ±6.0 | 25 | 2 (Fixed) | 12 | 55 | ±3.6 | 30 |
| | EL5108 | 1 | 450 | 4500 | ±2.25 | ±6.6 | 8 | ±1, 2 (Fixed) | 3.5 | 135 | ±3.8 | 5 |
| | EL5373 | 3 | 450 | 1100 | ±2.25 | ±6.0 | 25 | 2 (Fixed) | 12 | 55 | ±3.6 | 30 |
| | EL5308 | 3 | 450 | 4500 | ±2.25 | ±6.6 | 10 | ±1, 2 (Fixed) | 3.5 | 135 | ±3.8 | 5 |
| | EL5374 | 3 | 550 | 850 | ±2.25 | ±6.0 | 21 | 1 | 12 | 60 | ±3.8 | 25 |
| | EL5375 | 3 | 550 | 900 | ±2.25 | ±6.6 | 21 | 1 | 10 | 60 | ±3.8 | 16 |
| | EL5104, EL5105 | 1 | 700 | 3000 | ±2.25 | ±6.6 | 10 | 1 | 9.5 | 160 | ±3.8 | 10 |
| | EL5204, EL5205 | 2 | 700 | 3000 | ±2.5 | ±5 | 10 | 1 | 9.5 | 160 | ±3.8 | 10 |
| | EL5304 | 3 | 700 | 3000 | ±2.25 | ±6.6 | 10 | 1 | 9.5 | 160 | ±3.8 | 10 |

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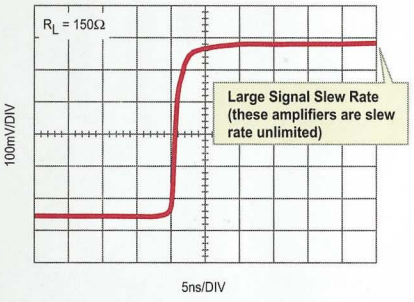


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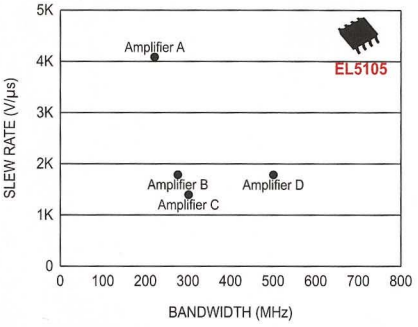


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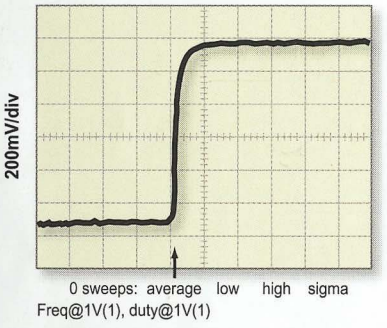


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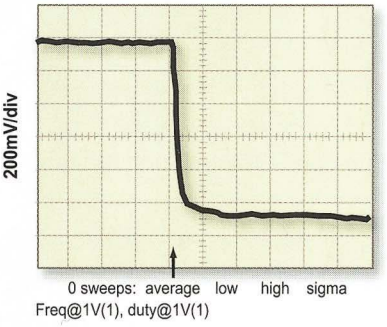


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- Low offset voltage: 10mV max
- Output current: 160mA
- $A_{VOL}$ = 1400
- Diff gain/phase: 0.01%/0.02°

| Device | # of Amps | BW @ -3dB (MHz) | Slew Rate (V/µs) | $V_S$ (min) (V) | $V_S$ (max) (V) | $V_N$ (nV/√Hz) | Gain $A_V$ (min) (V) | $I_S$ (per amp) (mA) | $I_{OUT}$ (mA) | $V_{OUT}$ (V) | $V_{OS}$ (max) (mV) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| EL5100 | 1 | 300 | 2200 | ±2.25 | ±6.6 | 10 | 1 | 2.6 | 100 | ±3.4 | 5 |
| EL5101 | 1 | 300 | 2200 | ±2.25 | ±6.6 | 10 | 1 | 2.6 | 100 | ±3.4 | 5 |
| EL5102 | 1 | 450 | 3500 | ±2.25 | ±6.6 | 13 | 1 | 5.3 | 140 | ±3.6 | 5 |
| EL5103 | 1 | 450 | 3500 | ±2.25 | ±6.6 | 13 | 1 | 5.3 | 140 | ±3.6 | 5 |
| EL5104 | 1 | 700 | 4500 | ±2.25 | ±6.6 | 14 | 1 | 9.5 | 160 | ±3.8 | 5 |
| EL5105 | 1 | 700 | 4500 | ±2.25 | ±6.6 | 14 | 1 | 9.5 | 160 | ±3.8 | 5 |
| EL5202 | 2 | 40 | 3500 | ±2.5 | ±6.6 | 13 | 1 | 5.3 | 140 | ±3.6 | 5 |
| EL5203 | 2 | 400 | 3500 | ±2.5 | ±6.6 | 13 | 1 | 5.3 | 140 | ±3.6 | 5 |
| EL5204 | 2 | 700 | 4500 | ±2.5 | ±5 | 14 | 1 | 9.5 | 160 | ±3.8 | 5 |
| EL5205 | 2 | 700 | 4500 | ±2.5 | ±5 | 14 | 1 | 9.5 | 160 | ±3.8 | 5 |
| EL5300 | 3 | 200 | 2200 | ±2.25 | ±6.6 | 10 | 1 | 2.6 | 120 | ±3.4 | 5 |
| EL5302 | 3 | 400 | 3500 | ±2.25 | ±6.6 | 13 | 1 | 5.3 | 140 | ±3.6 | 5 |
| EL5304 | 3 | 700 | 4500 | ±2.25 | ±6.6 | 14 | 1 | 9.5 | 160 | ±3.8 | 5 |

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# The right way to use instrumentation amplifiers

AVOID COMMON APPLICATION PROBLEMS WHEN CONNECTING REAL-WORLD SIGNALS TO INSTRUMENTATION AMPLIFIERS.

Instrumentation amplifiers find wide use in real-world data acquisition. However, designers often incorrectly apply them. Specifically, although modern in amps have excellent CMR (common-mode rejection), designers must limit the total common-mode voltage, plus the signal voltage, to avoid saturating the amplifier's internal input buffers. Unfortunately, they often overlook this requirement.

Other common application problems result from driving the in-amp reference terminal with a high-impedance source, operating low-supply-voltage in-amp circuits at gains that are much too high, ac coupling in-amp inputs without providing a dc return path to ground, and using mismatched RC-input-coupling components.

## A QUICK IN-AMP PRIMER

An in amp is a closed-loop-gain block with a differential input and a single-ended output. In amps also typically have a reference input that allows the user to level-shift the output voltage up or down. You use one or more internal or external resistors to set gain.

**Figure 1** shows a bridge-preamplifier circuit, a typical in-amp application. When sensing a signal, the bridge-resistor values change, unbalancing the bridge and causing a change in differential voltage across it. The signal output is this differential voltage, which connects directly to the in amp's inputs. In addition, under zero-signal conditions, a constant dc voltage is also present on both lines. This dc voltage is the same, or common mode, on both input lines.

In its primary function, the in amp normally rejects the common-mode dc voltage or any other voltage common to both lines, such as noise and hum, and amplifies the differential-signal voltage, the difference in voltage between the two lines.

## CMR: OP AMP VERSUS IN AMP

For many applications, CMR is essential for extracting weak signals in the presence of noise, hum, or dc-offset voltages. Op amps and in amps both provide some CMR. However, in amps prevent the common-mode signal from appearing at the amplifier output. Even though the op amp also has CMR, the common-mode voltage normally transfers to the output, at unity gain, along with the signal.

**Figure 2** shows an op amp connected to an input source (a bridge sensor). The bridge output is riding on a common-mode dc voltage. Because of feedback applied externally between the op amp's output and its summing junction, the voltage on the + input is the same as that on the − input. Therefore, the op amp ideally has 0V across its input terminals. As a result, the voltage at the op-amp output must equal $V_{CM}$, for 0V differential input.

In practice, the op amp's closed-loop gain amplifies the signal, and the common-mode voltage receives only unity gain. This difference in gain does provide some reduction in common-mode voltage, as a percentage of signal voltage. However, the common-mode voltage still appears at the output, and its presence reduces the amplifier's available output swing. For many reasons, any common-mode dc or ac signal appearing at the op amp's output is highly undesirable.

**Figure 3** shows the common three-op-amp in-amp circuit. A modern IC instrumentation amplifier, such as Analog Devices' AD8221, normally includes all of these components. As with an op amp, the input buffers of an in-amp circuit, $A_1$ and $A_2$, amplify the signal voltage, and the common-mode voltage receives only unity gain. But now, each buffer's output drives a

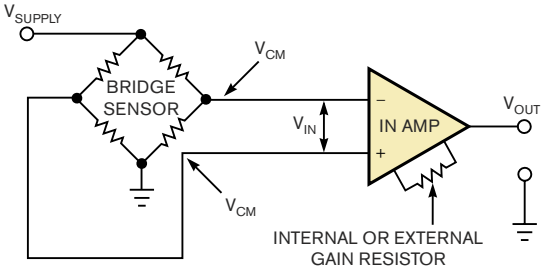



Figure 1 Designers can use instrumentation amplifiers in classic bridge circuits. Here, the dc common-mode voltage can easily be a large percentage of the supply voltage.

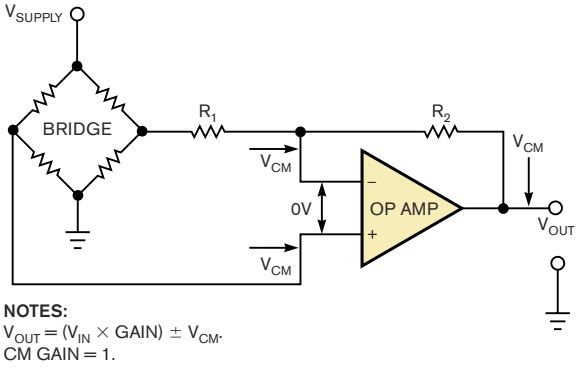



Figure 2 This inverting amplifier circuit uses an op amp. Here, both the signal voltage and the common-mode voltage appear at the amplifier's output.

subtracter circuit, $A_3$, which passes only the difference voltage and effectively rejects any common-mode voltages.

A common application problem that affects monolithic devices of the three-op-amp in-amp configuration occurs when dc common-mode input voltages render a single-supply in-amp circuit inoperative. Designers often correctly select a so-called single-supply in amp, so that they can operate the circuit from a low, single-supply voltage. But then they run into trouble.

For example, take the case of an in-amp bridge circuit operated from a 5V-dc single-supply voltage (**Figure 4**). Many designers simply ground the in amp's reference-input terminal, $V_{REF}$, as they normally would for dual-supply operation.

In this simplified case, with a bridge circuit using equal-value resistors, the buffers' (zero-signal) outputs ($A_1$ and $A_2$) are both 2.5V dc. This situation occurs because the in amp's buffers operate at unity gain for common-mode voltages. With both buffers applying the same 2.5V dc to the in amp's output-subtracter section, it tries to swing to 0V. In reality, even good "rail-to-rail" amplifiers cannot swing all the way down to the negative supply—in this case, "ground" or 0V—so a fairly large error already exists. Clearly, any signals from the bridge that would otherwise try to swing the in-amp output negative make no change at all. So, the circuit is basically nonfunctional, and an unwary designer may easily not notice this problem because the in amp's output appears to be about the same as it would be with no common-mode voltage applied.

A solution to this common problem is to apply half the supply voltage, 2.5V, to the in amp's reference pin, so that $A_3$'s output is centered at midsupply. The output can now swing both above and below this midsupply voltage. However, other things being equal, low-voltage, single-supply circuits typically have less dynamic range than their dual-supply cousins.

A similar problem occurs when low supply voltages and high amplifier gain render the in-amp circuit inoperative. It most commonly occurs when in amps are operating at high gains, such as 1000 (**Figure 5**). Under these circumstances, a 10-mV-p-p input times a gain of 1000 creates a 10V-p-p signal between the outputs of $A_1$ and $A_2$. When using ±15V supplies, this situation may be possible. However, the in amp will become nonfunctional if a 5V single or even a 5V dual supply powers the circuit. And, if the circuit is a bridge amplifier with its inherently high dc common-mode voltage, it adds further complications.

Because users of monolithic ICs do not have access to the buffer outputs, $A_1$ and $A_2$, they see what's happening only at the final output—the output of $A_3$. Again, this situation may result in a serious design problem that goes undetected, sometimes

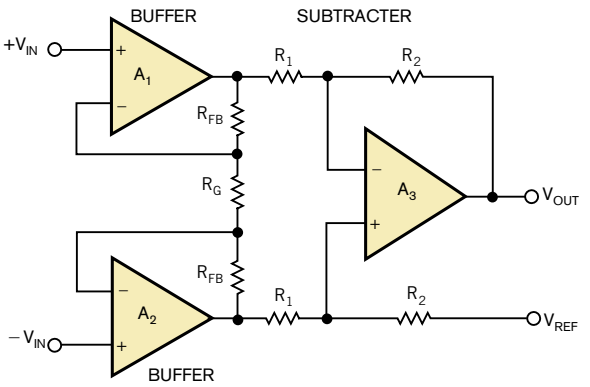



Figure 3 A common instrumentation amplifier employs three op amps.

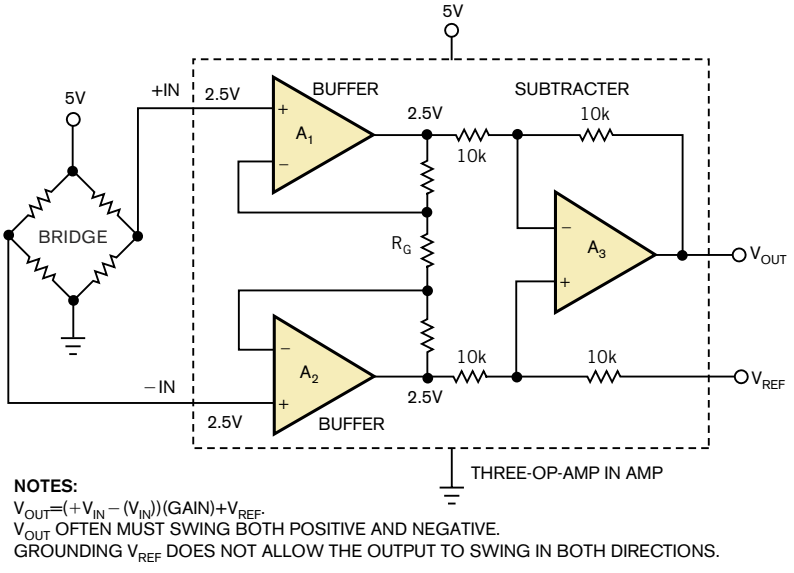
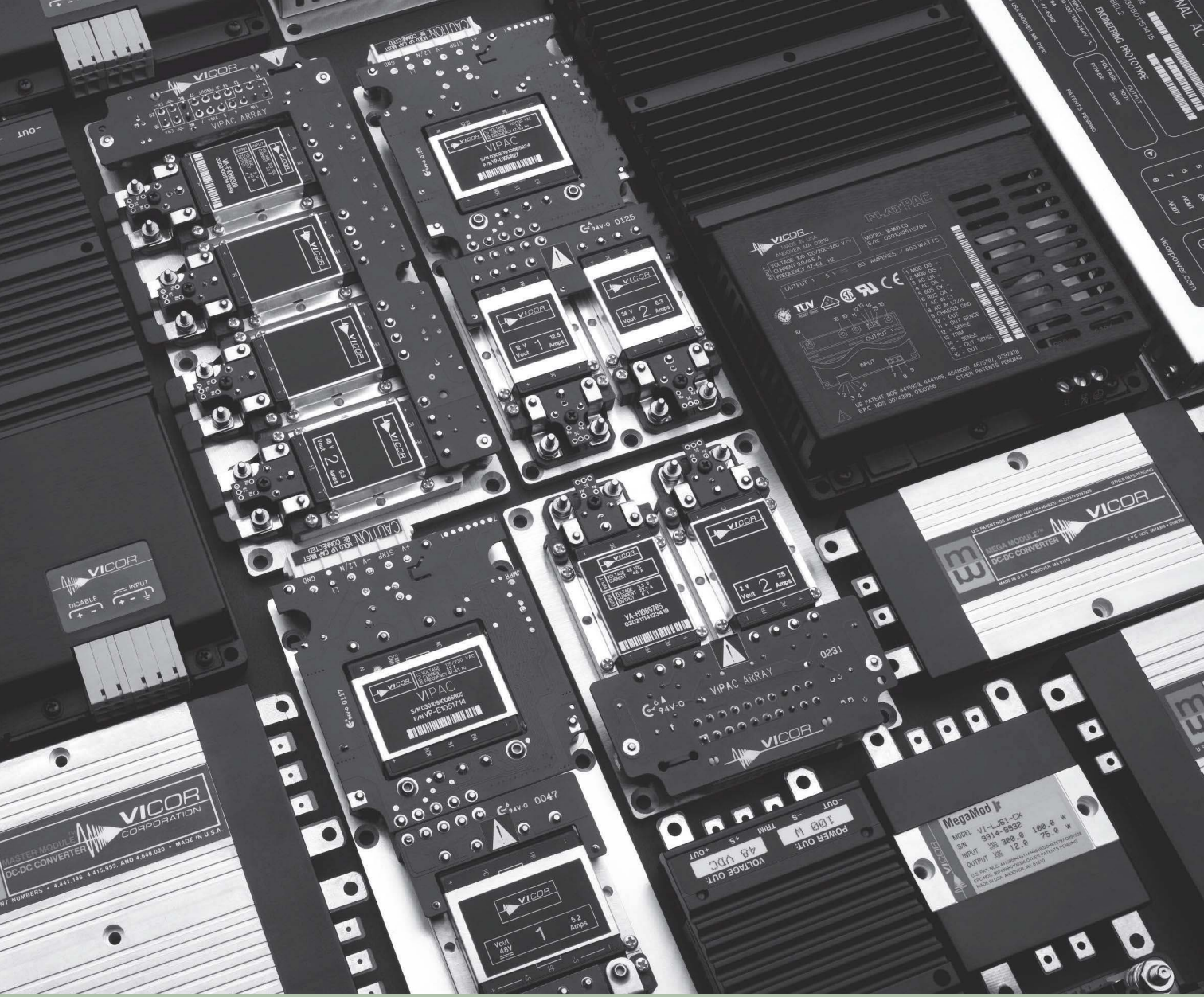



Figure 4 A three-op-amp in-amp circuit may exhibit a reduced common-mode-voltage range.

**TABLE 1 RECOMMENDED COMPONENT VALUES FOR AC COUPLING IN-AMP INPUTS**

| –3-dB low frequency roll-off (Hz) | RC-coupling components | | Input-bias current $I_B$ (nA) | $V_{OS}$ ($\Delta V_{CM}$) at each input | $V_{OS}$ error for 2% $R_1$, $R_2$ mismatch, assuming $I_{B1}=I_{B2}$ (µA) |
|---|---|---|---|---|---|
| | $C_1$, $C_2$ (µF) | $R_1$, $R_2$ (Ω) | | | |
| 2 | 0.1 | 1M | 2 | 2 mV | 40 |
| 2 | 0.1 | 1M | 10 | 10 mV | 200 |
| 30 | 0.047 | 115k | 2 | 230 µV | 5 |
| 30 | 0.1 | 53.6k | 10 | 536 µV | 11 |
| 100 | 0.01 | 162k | 2 | 324 µV | 7 |
| 100 | 0.01 | 162k | 10 | 1.6 mV | 32 |
| 500 | 0.002 | 162k | 2 | 324 µV | 7 |
| 500 | 0.002 | 162k | 10 | 1.6 mV | 32 |

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Another common application problem stems from operating standard, non-rail-to-rail devices, from low single-supply voltages. A high-quality rail-to-rail in amp, such as Analog Devices' AD623, can swing its output to within 0.5V of the positive-supply line and down to 0.01V above ground. Its input-voltage range is similar. Under these conditions, the amplifier's output swing almost equals the supply voltage. So, when using a 5V single supply, the amplifier has approximately a 4.49V output swing. Unfortunately, some designers forget about amplifier headroom and use standard, non-rail-to-rail products in these applications. Even a good dual-supply in amp has an output swing within only about 2V of either rail. So, using a 12V single-supply voltage, with the in amp's output centered on 6V, a rail-to-rail amplifier could swing ±5.5V, but a standard product would have only ±4V output swing (11V p-p versus 8V p-p).

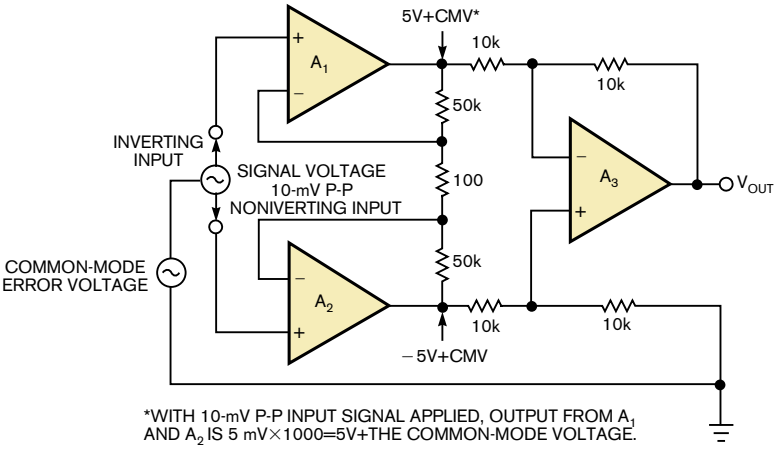


Figure 5 High gain and low supply voltages can result in buffer-amplifier clipping.

Yet another common application problem occurs when designers try to drive the reference pin of an in amp with a high-impedance source. Typical values for the impedance of the reference input in many popular in amps are 20 to 125 kΩ. If a low-impedance source, such as an op amp, is directly driving the reference, there is no problem. But often, an unwary designer tries to use a resistive voltage divider as a low-cost ratio-metric reference and ends up introducing serious errors (**Figure 6**).

The reference input is part of the output-subtracter circuit in a typical three-op-amp instrumentation amplifier. As such, it has a finite input resistance, approximately equal to $R_{REF1}$ plus $R_{REF2}$—usually, $2\times R_{REF}$. Adding external resistor $R_2$ between the reference terminal and common unbalances the $A_3$ subtracter circuit, introducing a CMR error. An obvious way to minimize this problem is to reduce the value of $R_2$ to approximately 0.1% of $R_{REF1}$ plus $R_{REF2}$ (for 60-dB CMR). However, with 10-kΩ values of $R_{REF1}$ and $R_{REF2}$ (20,000 total input Z), $R_2$ needs to be 20Ω. This value, in turn, unnecessarily burns large amounts of supply current in the voltage-divider network. There is also the issue of $R_{REF1}$ and $R_{REF2}$'s shunting $R_2$ and causing a reference-voltage error.

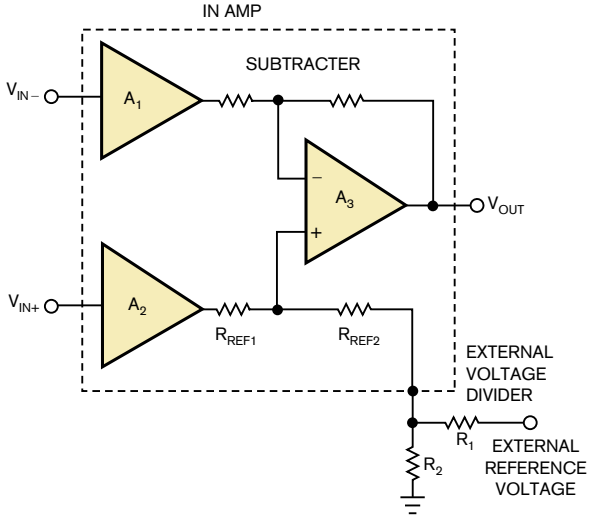


Figure 6 Driving the reference input from a high-Z source can introduce errors. In this case, $R_2$'s resistance causes a CMR error as $R_{REF1}$ and $R_{REF2}$ are now unbalanced. The shunting of $R_2$ by $R_{REF1}$ and $R_{REF2}$ introduces an additional voltage-reference error.

Together, these errors present a strong case for the use of an op-amp buffer to drive the reference pin (**Figure 7**). The op amp has a low output impedance—typically less than1Ω—and consequently does not contribute any significant CMR error. Note that using two 1% resistors in this application can produce as much as 2% gain error due to resistor mismatch.

Limits on dc CMR and the fact that many circuits do not require a true dc response tempt designers to ac couple the inputs of in-amp circuits. A common, incorrect procedure is to simply connect a suitable capacitor in series with each in-amp input terminal (**Figure 8**).

Again, because a monolithic in amp is a complete package, designers often fail to realize what is inside the IC. In amps thus connected with these "floating" inputs have no dc reference. The input bias currents charge up the ac coupling capacitors, $C_1$ and $C_2$, until they exceed the input common-mode voltage.

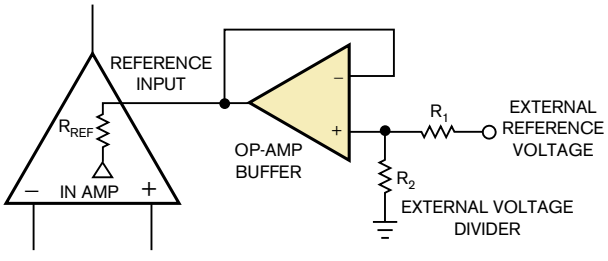


Figure 7 Adding an op-amp buffer amplifier isolates the in amp's reference terminal from the voltage divider.

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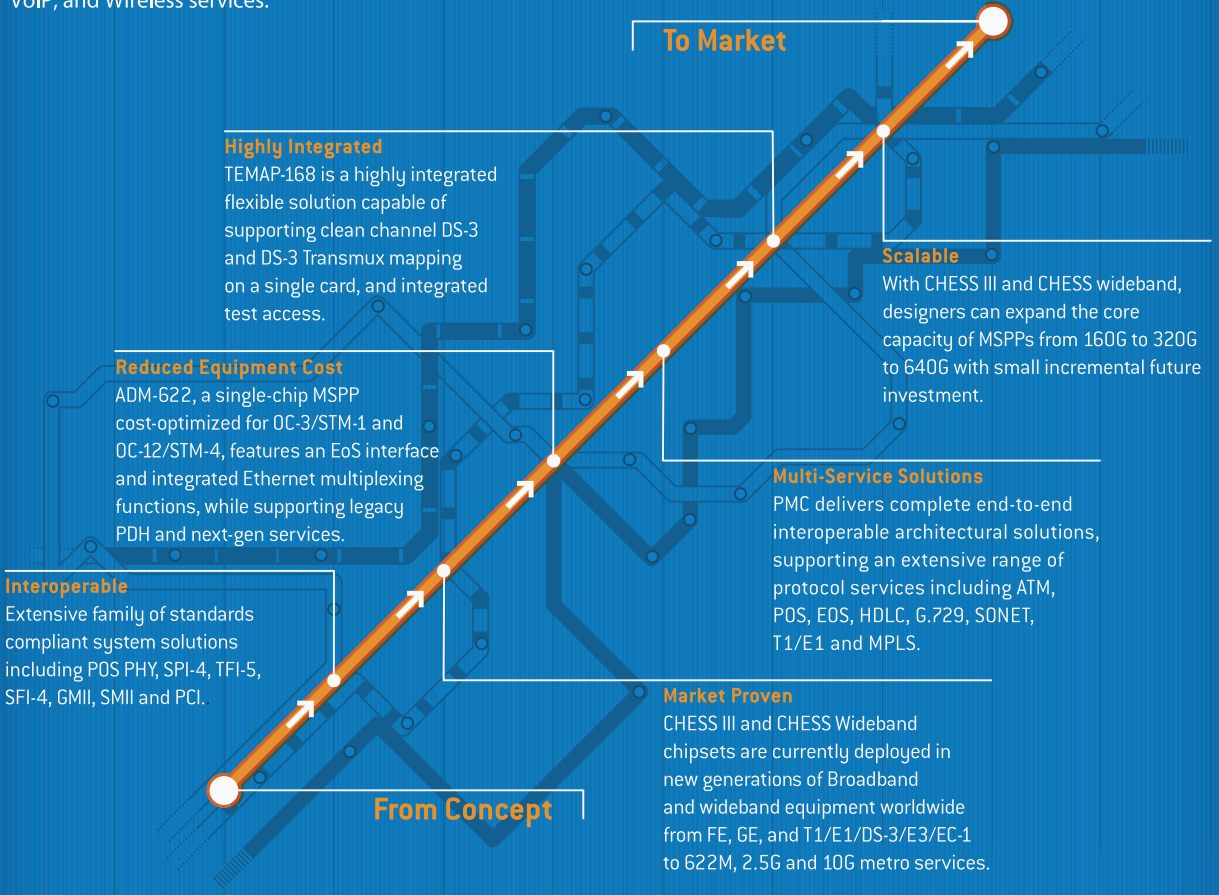


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In other words, the capacitors charge up to the supply line or down to ground, depending on the direction of the input bias currents. With a FET input device and high-value capacitors, it could take several minutes before the in amp becomes inoperative. Therefore, a casual lab test might not detect this problem, so it's important to avoid it altogether. Fortunately, for dual-supply operation, a simple solution exists: Just add two large-value dc return resistors, one between each input and ground (**Figure 9**). Now, both inputs are dc-referenced to ground and move only when an input signal drives them.

Using an in amp powered by a single supply, ac coupling is more complicated and normally requires applying a dc common-mode voltage, $V_{CM}$, to both inputs (**Figure 10**). This step is necessary, because the in amp's output cannot swing below the negative supply—in this case, ground. Here, if the in amp's output voltage tries to swing more than a few millivolts negative, the signal is clipped.

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Choosing appropriate voltages for $V_{CM}$ and $V_{REF}$ is the next important design consideration, especially in low-supply-voltage applications. In general, set $V_{CM}$ to the middle of the expected input dynamic range and center $V_{REF}$ on the expected output dynamic range. As an example, say that the expected input signal (−IN−(IN)) is +1V to −2V. Under these conditions, the in amp's input buffers need to swing both positive and negative with respect to $V_{CM}$. Therefore, you must raise $V_{CM}$ above ground for this scenario to happen. Assume that the in amp is operating at unity gain. Setting $V_{CM}$ to 2V or a bit higher allows 2V of headroom in the minus direction. The trade-off is that there is now 2V less swing in the positive direction. If the in amp is operating with gain, tailor $V_{CM}$ to allow the buffer outputs to swing fully without clipping.

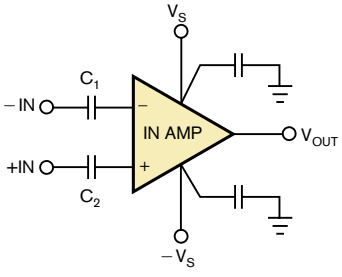


Figure 8 An incorrect procedure results in this nonfunctional, ac-coupled in-amp circuit.

Output centering is similar: Estimate the amount and direction of the in amp's output swing—in most cases, $V_{IN}\times gain+V_{CM}$—and then apply a reference voltage at $V_{REF}$ that is in the center of that range.

The choice of dc-return-resistor value for ac-coupled circuits is a trade-off between offset errors and the physical and electrical size of the input coupling capacitors. The larger the value of the input resistor, the smaller the required input coupling capacitor. This approach saves both money and pc-board space. However, the trade-off is that high-value input resistors increase the offset-voltage error due to input offset currents. Offset-voltage drift and resistor noise also increase.

With lower resistor values, higher value input capacitors for $C_1$ and $C_2$ are necessary to provide the same −3-dB corner frequency. That is: $F_{-3\,dB}=(1/(2\pi R_1C_1))$, where $R_1=R_2$ and $C_1=C_2$.

Unless a large enough dc voltage is present on either side of the ac coupling capacitor, use nonpolarized capacitors. Some capacitors, such as electrolytics, function as diodes if you do not properly dc-bias them. In the interest of keeping components

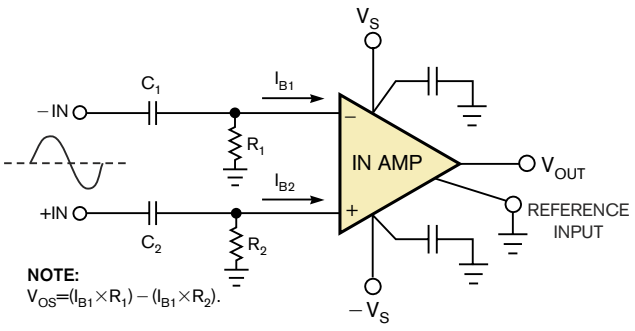


Figure 9 For dual-supply operation, a high-value resistor connected between each input and ground provides the necessary dc return path.

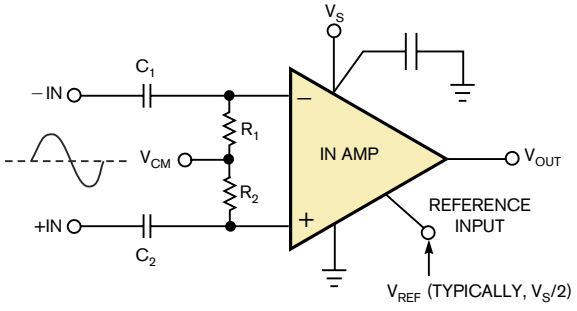


Figure 10 An ac-coupled, single-supply in-amp circuit normally requires a dc common-mode voltage, $V_{CM}$, applied to both inputs.

as small as possible, select capacitors of 0.1 µF or less. Generally, the lower the capacitor value, the less costly and smaller the capacitor is. The voltage rating of the input coupling capacitor needs to be high enough to avoid breakdown from any high-voltage input transients that might occur. One final word of caution: Avoid high-K (high-dielectric-constant) ceramic capacitors, which can introduce harmonic distortion.

When ac coupling, any mismatch between the two dc return resistors causes an input offset imbalance ($I_{B1}-I_{B2}$), which creates an input offset-voltage error (**Figure 9**). **Table 1** gives R and C cookbook component values for various circuit bandwidths and the $V_{OS}$ error for two levels of input-bias current. EDN

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1. Kitchin, Charles and Lewis Counts, *A Designer's Guide to Instrumentation Amplifiers, Second Edition*, available free from Analog Devices at www.analog.com/analog_root/static/technology/amplifiersLinear/InstrumentationAmplifiers/designersGuide.html.


## AUTHORS' BIOGRAPHIES


*Charles Kitchin is a hardware applications engineer for Analog Devices (Wilmington, MA). His main responsibilities include writing technical publications and developing applications circuits. He has published more than 80 technical articles and design ideas, three books, and numerous application notes.*

*Lew Counts is the vice president of the Advanced Linear Products Division of Analog Devices and was promoted to division fellow, one of Analog Devices' highest awards, in 1984.*

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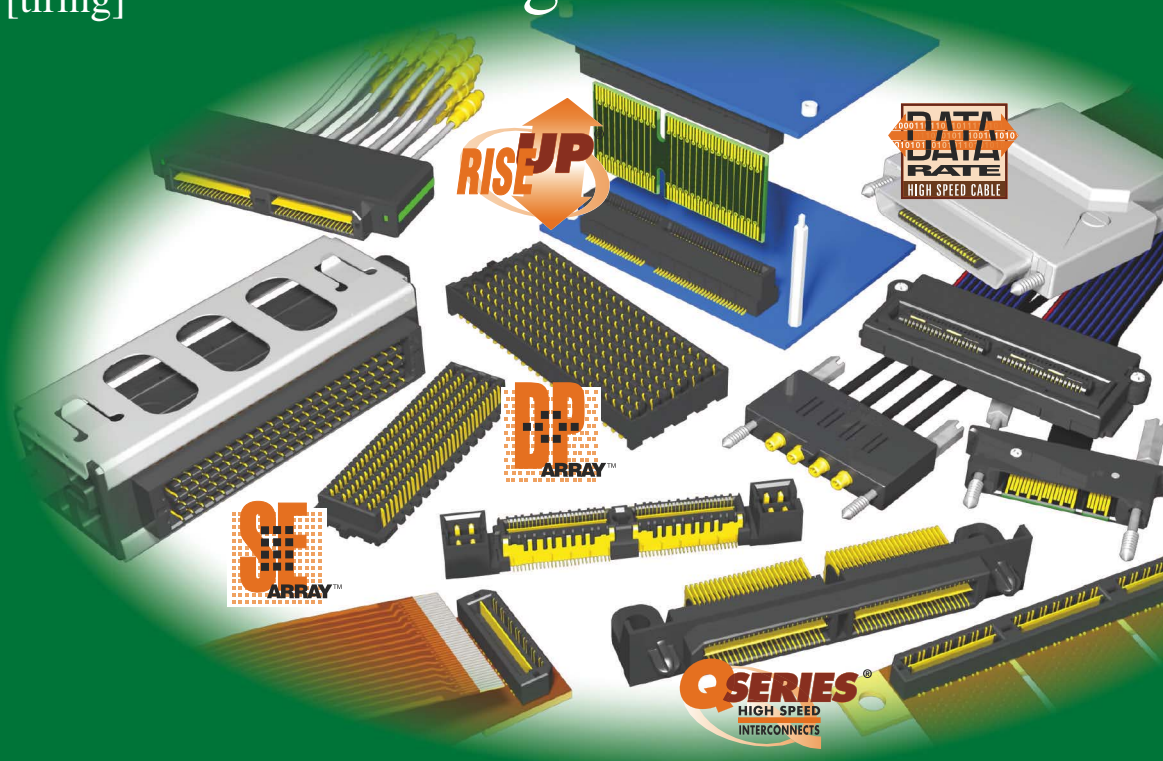


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# In search of cool computing

## MULTIPROCESSOR-CHIP DESIGNS HEAD DOWN A BLIND ALLEY OF POWER AND HEAT PROBLEMS.

The biggest challenge facing SOC (system-on-chip) designers today is how to deliver higher performance and minimize IC power and the attendant heat. Power and cooling needs are pushing the limits of available technology and creating budgetary strains for users—both for the initial upgrades of power and cooling systems and for their ongoing energy costs. But in their attempts to solve these challenges, many chip designers have headed down a blind alleyway.

Many previous- and current-generation processors rely heavily on ILP (instruction-level parallelism) to speed single-threaded applications. ILP attempts to increase performance by determining, in real time, instructions that can execute in parallel.

In their newest designs, chip developers are increasingly turning to CMPs (chip multiprocessors)—multiple processors on a single silicon die that reduce power demands and improve efficiency by sharing on-chip structures, such as memory controllers, between the cores versus two separate chips.

**THE AGGREGATE THROUGHPUT IS FIVE TO 15 TIMES BETTER THAN CONTEMPORARY PROCESSORS.**

However, these designs continue to rely on pipelines that were designed to deliver performance gain by trying to attain high ILP. In doing so, the designs ignore the main characteristic of commercial applications (that is, large databases and CRM): They are rich in threads but poor in ILP. As a result, this strategy continues down the path of poorly matching workloads to the appropriate design and results in an even-less-power-efficient system.

At first glance, it appears that improving processor performance and lowering processor power demands are at odds, but this doesn't have to be the case. Multithreading—running multiple threads per processor core—hides the frequent high-latency events and exploits the thread-level parallelism common in commercial applications. By combining simple core CMPs with multithreading, it is possible to design processors that consume less power and deliver higher throughput. These single-chip processors exploit thread-level parallelism by employing fine-grained multithreading. This approach, CMT (chip multithreading), is ideal for commercial applications.

Under this design, the CMT processor has multiple independent 64-bit execution pipelines (cores). Each core can select from multiple active threads. The result is a processor that allows dozens of threads or processes to execute simultaneously on a single chip. The aggregate throughput of this design is approximately five to 15 times better than contemporary processors such as the Intel Xeon, AMD Opteron, and Sun UltraSPARC III.

Despite the far-greater throughput, the power density of this design is much less than other contemporary processors, making it better suited for dense rack-mount installations in the data center. As transistor density and processor complexity have increased over the past decade, power has shot upward. Although typical processors today often have a power density greater than 70W/cm$^2$, CMT designs can produce faster throughput with a power density in the range of 10 to 20W/cm$^2$.

### ILP VERSUS CMT

Most multicore chip designs aimed at the high-volume, horizontally scalable commercial-server market employ pipeline designs primarily targeting desktop (single-threaded or ILP-focused) applications. Designers then modify cache and interface architectures to support a coherent shared memory across two-, four-, and eight-processor systems, and they reduce the operating frequency and voltage for low power consumption. These designs attempt to execute instructions from a single thread in parallel (ILP) and typically have the following characteristics:

- superscalar designs that attempt to increase instructions per clock and require multiple independent execution units with dependency checking, scoreboarding, complex bypassing datapaths, and complex register files;
- 2.2- to 3.6-GHz clock frequencies, which demand hot, fast, and leaky transistors as well as power-hungry dynamic-circuit designs;
- pipelines with as many as 30 pipe stages from instruction fetch to retirement, requiring aggressive branch prediction and a vast number of state devices;
- out-of-order execution with wide instruction-issue windows, reorder buffers, and a variety of memory-speculation techniques; and
- multilevel caches—three and four levels, in some cases—to further combat memory latency.

With these designs, a serial and highly dependent instruction stream with little ILP limits performance on a typical commercial application. These features become power-consuming burdens when executing code lacking ILP and high in cache misses.

By contrast, CMT designs achieve high throughput by employing a fine-grained, multithreaded pipeline design. This

design suits applications with thread-level parallelism. Performance-enhancing features include:

- multiple independent, single-issue, in-order pipelines, each with a relaxed clock frequency, which require no extra transistors or power for multiple-issue or out-of-order execution;
- no branch prediction;
- a limited number of stages in the core pipeline (about a half-dozen stages, compared with as many as 30 on ILP designs);
- large, highly banked, on-chip secondary cache, which handles most memory requests to avoid incurring external DRAM power; and
- integrated I/O and DRAM controllers, which extract more performance and avoid powering external components and associated buses.

## OTHER POWER-THROTTLING TECHNIQUES

Designers can enhance the power-saving nature of the basic CMT architecture through additional hardware features that target two sources of high power consumption. Upon detecting that a chip is reaching a certain power limit, designers can use certain mechanisms to throttle down the power. Designers can gain additional power savings by reducing the issue rates of the cores and limiting activity in main memory.

Issue rates—the number of instructions that the processor can send down the pipeline in a certain period of time—can throttle back within the cores by putting specific threads in a sleep mode when power and thermal conditions exceed designated thresholds. When power and thermal conditions return to normal, threads resume executing instructions. You can use an external thermal diode to constantly translate the operating temperature into a voltage level that the processor will interpret.

Away from the core pipeline, another significant opportunity for power throttling lies in time-shared memory controllers. A high-performance CMT requires multiple next-generation memory controllers such as DDR2 memory channels to supply the necessary data. These controllers connect to tens or hundreds of DRAM chips and are therefore important contributors to power dissipation.

Under peak periods, software-enabled control registers can limit the number of open pages in the DDR memories. This approach throttles the rate at which reads and writes are issued, resulting in a reduction of both interface power and peak operating power with the DRAM devices.

## SOFTWARE REDUCES POWER CONSUMPTION

Designers can achieve additional reductions in power consumption on the operating-system layer. Idle loops occur more frequently than you might expect, especially on a processor with 32 or more threads. To reduce power consumption, the operating system can halt a thread when it enters an idle loop, resuming execution only when it is ready to schedule work. This situation not only helps with power reduction, but also limits interaction with other active threads on that core.

Thread-scheduling algorithms are also important tools. Although it is difficult for an operating system to gauge how a workload might behave, it can follow guidelines about how best to spread distinct workloads across multiple cores. The operating system can localize threads and processes, having some amount of affinity—for example, the same process with different data—by assigning them to the same core or to a nearby core. If there are 16 active lightweight processes, it is beneficial from a power perspective to concentrate those threads on four cores as opposed to spreading that load across eight cores.

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## A NEW ERA

Chip multithreading will enable a new era of cool computing, delivering an unprecedented combination of high throughput and low power consumption. Chip designers who pursue higher performance with the traditional ILP techniques will fall further behind the performance/power-consumption curve. EDN

## AUTHOR'S BIOGRAPHY

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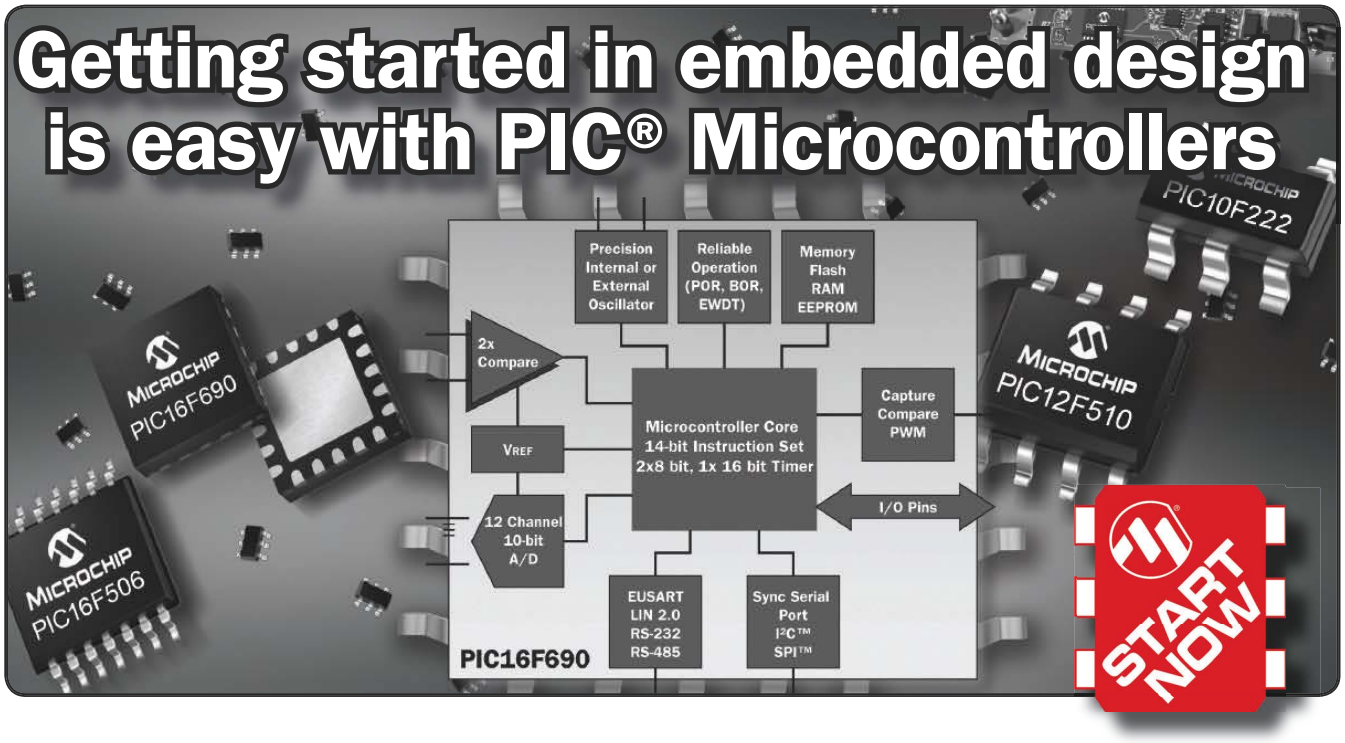


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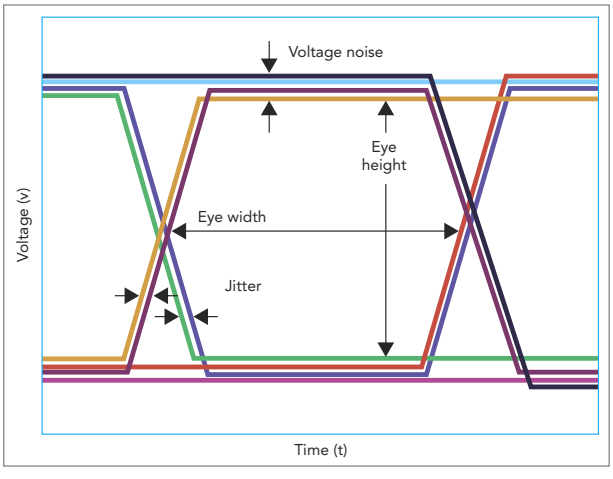
# THE DATA DETECTIVE

# Digital Signals Arrive on Time

Clock signals comprise rising edges (logic-low to logic-high transitions), and falling edges (logic-high to logic-low transitions). A clock signal can exist as square waves with a regular period and duty cycle or as a continuous series of periodic pulses. The latter type of signal can trigger a latch to accept data, interrupt a microcontroller, and so on. Regular clock waveforms govern the timing of microprocessor-based controllers, communication systems, memory chips, and other devices that perform operations at regular intervals. Depending on the clocked device, either a rising or a falling clock-signal edge causes an action. A device such as a double data-rate (DDR) memory uses both clock edges to trigger actions.

Clock signals do not cause instantaneous actions, though. A memory device, for example, requires the presence of unchanging data during a fixed amount of time, called the set-up time ($t_{su}$), prior to the arrival of a clock signal. The data must then remain stable for a specified hold time ($t_H$) after the clock-edge transition. These times, specified in chip manufacturers' data sheets, ensure designers know the timing requirements for the data and clock signals input to a device. A hand-drawn timing diagram may show the theoretical action of clocked circuits, but the design of complex circuits requires simulations that account for timing values such as $t_{su}$ and $t_H$.




**In this eye diagram, the overlaid samples of all 3-bit states show how jitter and voltage noise appear on a clock signal. Many communication signals must conform to standard templates that define minimum eye values (colored lines exaggerated for emphasis).**

Unfortunately, clock signals come with imperfections such as jitter and drift. Drift occurs when the period of two clocks differs slightly over time. These slight timing differences can accumulate and affect a system adversely. For example, assume researchers have two data-acquisition devices that each supply a 100-MHz clock. Even if the two devices are synchronized to start together perfectly, over time one device may begin to run slightly faster than the other due to circuit imperfections or due to an external factor such as temperature. That difference badly skews the data the researchers expect will align perfectly in time. Timing techniques can reduce or eliminate drift.

Jitter represents a slight deviation in the timing of a signal's edges during a clock cycle, and it can arise from signal cross-talk, switching transients, and the effect of other signals. Engineers generally measure jitter as a time difference between the clock signal of interest and a reference clock signal at their zero-crossing points. Jitter measurements range from a visual estimate on an oscilloscope to quantitative measurements that extract statistical data from many signal samples.

The sequential acquisition of a clock signal over three periods produces a diagram that reveals both jitter and voltage noise. Because the signal may produce any of eight binary patterns during an acquisition, a measuring instrument overlays millions of signal samples to create an "eye" diagram (see figure). The overlay diagram lets engineers determine a signal's maximum jitter and voltage noise. As these errors increase, the eye width and height decrease. The better the quality of a digital signal, the more open the eye. Said differently, engineers strive to maximize eye width and height.

When an eye diagram comprises millions of samples, the eye width indicates the time the data lines remain stable. Thus, engineers can determine how much set-up and hold time a clock signal provides.

## A Case of the Jitters?

The microcontroller board Jane designed seems to suffer from intermittent problems. The microcontroller's specifications list tight timing requirements, so the cause of intermittent behavior may rest with Jane's new clock circuit.

Can you help Jane analyze her clock signal to identify possible problems?

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Go to http://rbi.ims.ca/4396-502 to solve the challenge!

BY PETE COLLINS • JTAG TECHNOLOGIES

# Extensions to the IEEE 1149.1 boundary-scan standard

DESPITE THE SUCCESS OF THE IEEE 1149.1 BOUNDARY-SCAN STANDARD, ACCEPTANCE OF THE 1149.4 MIXED-SIGNAL EXTENSION HAS BEEN SLOW. THE INDUSTRY BADLY NEEDS THAT EXTENSION AND OTHERS, HOWEVER, AND SEVERAL COMPANIES ARE HARD AT WORK TO PUT THEM ON THE FAST TRACK.

The IEEE 1149.1 boundary-scan standard was developed almost 15 years ago to resolve the problems associated with limited physical access for probing test points on pc boards and to verify that device pins have been soldered correctly and are free of solder shorts and open circuits. However, the test industry now faces new problems that nobody envisioned when the standard was developed back in 1990, and a number of working groups have engaged in a sustained effort to develop new standards that build on the success and acceptance of IEEE 1149.1.

More recent standards that extend 1149.1 are 1149.4, the mixed-signal test-bus standard for testing analog pins; 1149.6 for testing the interconnections between ac-coupled differential nets; and IEEE 1532 for the in-system configuration of programmable devices.

The 1149.4 standard specifies that every signal pin must be associated with a boundary module, which in the case of the digital pins is referred to as a DBM (digital-boundary module). DBMs are identical to the boundary-scan cells defined in 1149.1. Mixed-signal pins are associated with ABMs (analog-boundary modules). Each ABM consists of a switching network that allows the mixed-signal pin to be disconnected from the core circuitry in the CD (core-disconnect) state and allows it to connect to the internal bus or the internal dc reference voltages. Alternatively, if the PROBE instruction is selected, the network leaves all pins in functional mode and allows the pins' signal to be measured via the internal analog bus (**Reference 1**).

**Figure 1** shows the construction of a simple mixed-signal device that consists of several DBMs and ABMs, which are selected through the TAP (test-access port), as defined by 1149.1, and an ATAP (analog test-access port), which supports 1149.4's analog stimulus-and-response capabilities. This arrangement requires two extra AT (analog-test) pins: $AT_1$ for providing an external test stimulus and $AT_2$ for routing signals connected to the associated ABMs to external measurement instrumentation.

The external analog-test bus, which connects to $AT_1$ and $AT_2$, accesses an internal bus under the control of the TBIC (test-bus interface circuit). The TBIC allows the internal test-bus

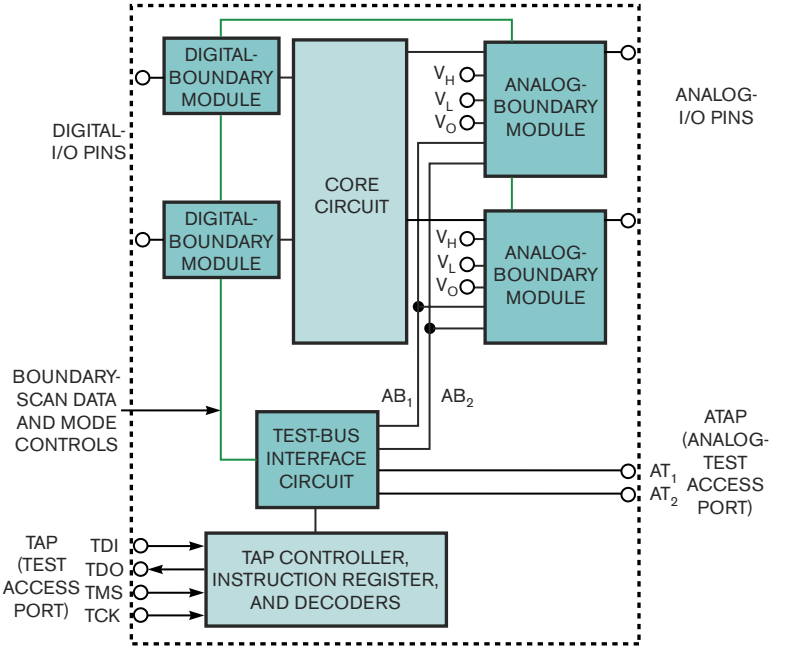



Figure 1 In this simple chip, boundary-scan features surround the core.

lines to connect to either or both ATAP pins, isolates the internal test bus when it is not in use to eliminate unwanted noise interference, or connects the bus to one of two dc voltages ($V_H$ and $V_L$), which act as logic values for performing standard dc interconnect testing (**Figure 2**).

## CONTROLLING ABMs

A 4-bit register controls each ABM. The register is part of the boundary-scan data register and can capture digital-test results that represent either logic values or digitized analog responses. As can the DBMs, the individual control registers can load and unload through the 1149.1 TAP.

The four bits are C, D, $B_1$, and $B_2$ (control, data, $ABUS_1$, and $ABUS_2$). The C bit acts as an enable pin, and the D bit provides the pin's logic values, $V_H$ and $V_L$. When the C and D bits are both zero, the pin is disconnected from the core through the CD switch. $B_1$ and $B_2$ control the switches that connect the signal pin respectively to the $AB_1$ and $AB_2$ test-bus lines.

The 1149.4 standard requires support for one more instruction than those for which 1149.1 mandates support. This instruction is PROBE, whose primary purpose is to allow real-time access to signal pins without affecting the UUT's (unit under test's) normal operating mode. In effect, the PROBE instruction is similar to SAMPLE/PRELOAD and allows virtual probing of selected IC pins without impacting their normal function.

At the board level, a single boundary-scan path can link any combination of 1149.1- and 1149.4-compliant devices, with the TDO (test-data-out) pin of one device connected to the TDI (test-data-in) pin of the next. The TCK (test-clock) and TMS (test-mode-select) pins connect in parallel as defined in 1149.1. Similarly, the $AT_1$ and $AT_2$ pins connect in parallel to the 1149.4-compliant devices (**Figure 3**).

## DEVELOPMENTS

Although 1149.4 was approved in June 1999, the industry has been slow in adopting it. More important, IC vendors have been slow to produce devices that would enable board designers to use and experiment with the technology. To stimulate interest in implementing 1149.4, National Semiconductor (**Reference 2**), an innovator in analog semiconductors, and LogicVision, a provider of embedded-test intellectual property for ICs and systems, collaborated on developing the first general-purpose IEEE 1149.4-compliant IC, the STA400 (**Figure 4**).

The STA400 is mainly an evaluation chip whose core functions primarily as a simple analog multiplexer comprising 11 ABMs that can connect to circuit nodes to enable injection of a test stimulus or monitoring of discrete dc voltages and ac signals. You can use the chip to determine values of discrete passive components by injecting currents at different signal nodes, measuring the resultant voltage at each node, and calculating the value of the selected components.

JTAG Technologies has developed an IEEE 1149.4 evaluation kit that uses STA400s to let users select circuit nodes and perform resistance, capacitance, voltage, ac-signal, and characteristic-impedance measurements on an evaluation board

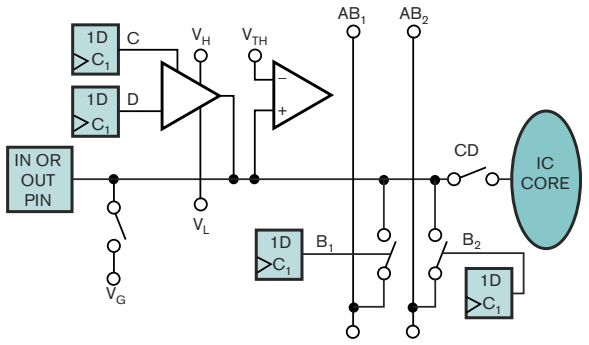



Figure 2 This analog-boundary module resides on an IEEE 1149.4 IC and allows you to connect an I/O pin to the IC's core or to either of two analog buses.

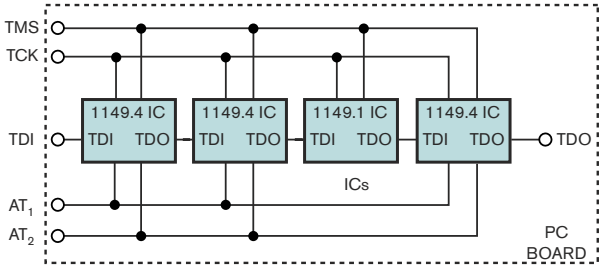
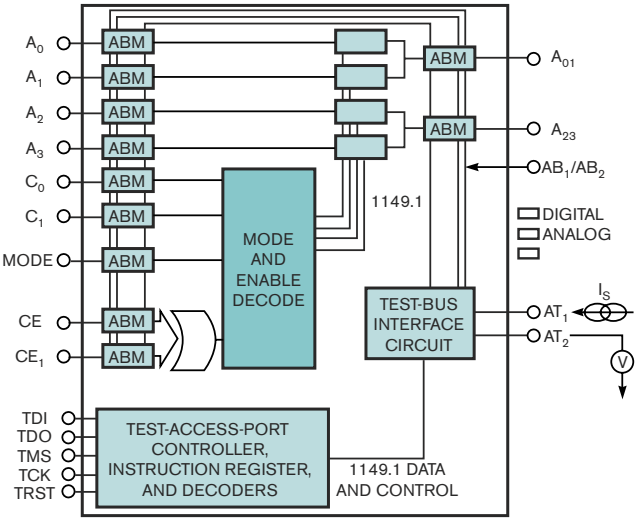



Figure 3 On the pc board, the analog-test buses, $AT_1$ and $AT_2$, connect to multiple ICs.




NOTE:
ABM=ANALOG-BOUNDARY MODULE.

Figure 4 The STA400 evaluation chip allows you to experiment with 1149.4-based test concepts.

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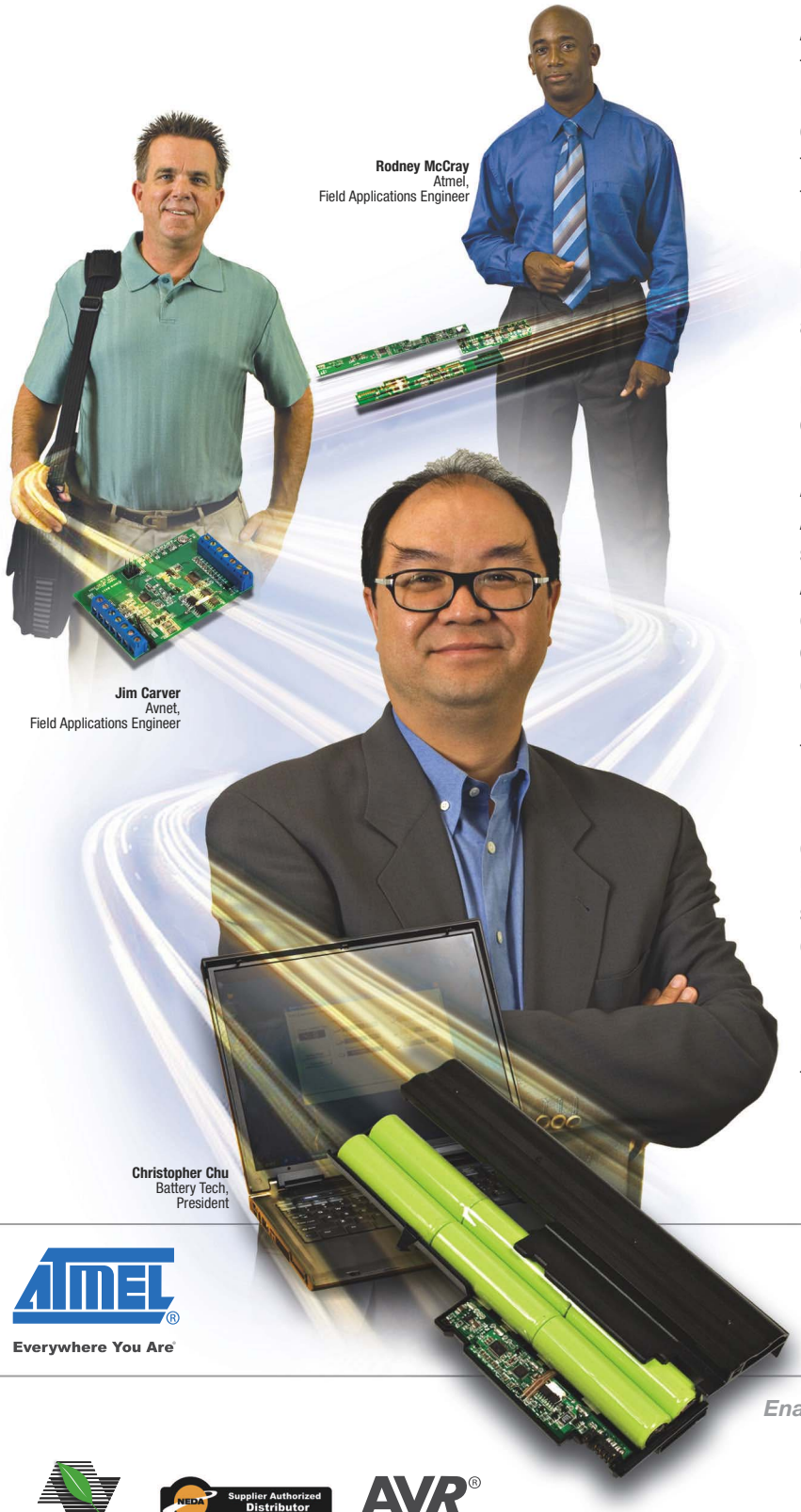
BTI has also charged Avnet and Atmel to move its existing designs to Atmel's AVR platform – the industry's leading flash-based microcontroller. It's no shock to see why – with Avnet and Atmel's focused energy, BTI found total support across the board.

For additional application solutions and to download the BTI case study, visit: www.em.avnet.com/atmel/satb

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using a graphical user interface. In another application of this system, you can perform analog measurements on target boards by using the test resources (stimulus and measurement instrumentation) of the JTAG-1149.4 Explorer package (**references 3** and **4**).

## AC-COUPLED DIFFERENTIAL NETS

IEEE 1149.6 was developed to address the requirements of boundary-scan testing of ac-coupled differential nets. Coupling capacitors on high-speed digital interconnects block dc signals and prevent receivers from detecting them. Using an R-C network causes signals to decay over time, typically requiring at least 2.5 TCK cycles between driving a net and capturing a signal.

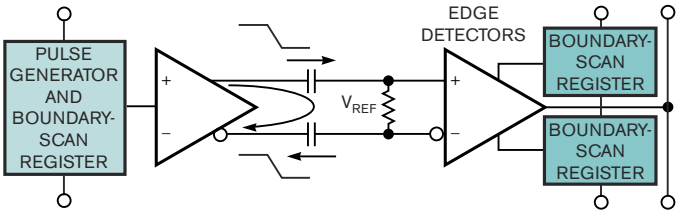
The basic implementation of 1149.6 requires adding to the signal-path driver a generator that can transmit a single pulse or a train of pulses depending on whether the EXTEST_PULSE or EXTEST_TRAIN instruction is loaded into the 1149.1 instruction register. A test receiver located behind the receiving-device pins detects a steady-state level or captures edge transitions (**Figure 5**). The test receiver must be able to support both of these new instructions as well as the traditional static 1149.1 EXTEST. When the IEEE 1149.1 EXTEST instruction is active, the receiver must revert to level sensing, whereas, when one of the new 1149.6 instructions is active, the receiver must capture edge transitions.

When the interconnection between the driver and the receiver is dc-coupled, the receiver must detect levels by referencing the input signal to a dc-bias voltage that the ac-mode-control signal selects (**Figure 6**). When the interconnection between the driver and the receiver is ac-coupled, the transitions at the receiver's input pins are detected by comparing the input signal with a delayed version of itself. In this self-referencing technique, the lowpass filter provides the signal delay. In **Figure 7**, the upper comparator detects rising edges, and the lower comparator detects falling edges. These comparator outputs respectively set and clear the receiver flip-flop, reproducing the original waveform at output C regardless of whether the input signal, A, is dc- or ac-coupled.

With the proliferation of multigigabit-per-second serial-data-communication protocols, a significant number of devices will likely implement 1149.6. In fact, several 1149.6-enabled devices are already available (**Reference 5**), and tools are in development to enable 1149.6 insertion and verification. Vendors are also upgrading board-test software to enable testing of 1149.6 components and their interconnections to other onboard boundary-scan-compliant devices.

## IN-SYSTEM PLD CONFIGURATION

For many years, the test industry has been asking for some level of standardization for ISC (in-system con-




**NOTES:**
PULSE GENERATOR AND BOUNDARY-SCAN REGISTER SUPPORT IEEE 1149.1 INTERCONNECT AND OFFER EDGE GENERATION/DETECTION FOR AC-COUPLED TESTS.

Figure 5 IEEE 1149.6 allows you to use boundary-scan technology to test such differential analog structures as drivers and receivers for ultrahigh-speed serial buses.

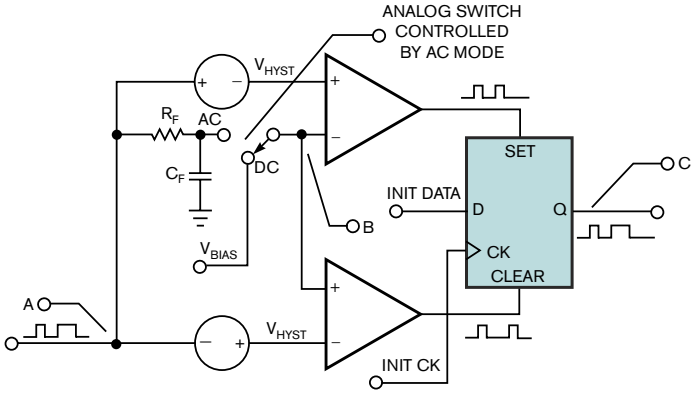



Figure 6 In this circuit, when the interconnection between the driver and the receiver is dc-coupled, the receiver must detect levels by referencing its input to a dc-bias voltage that the ac-mode-control signal selects.

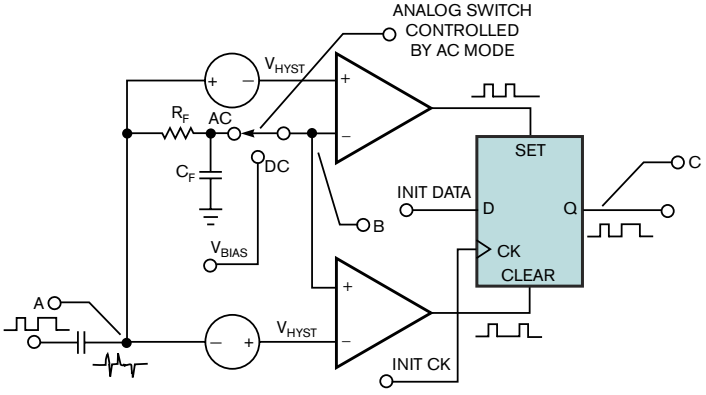
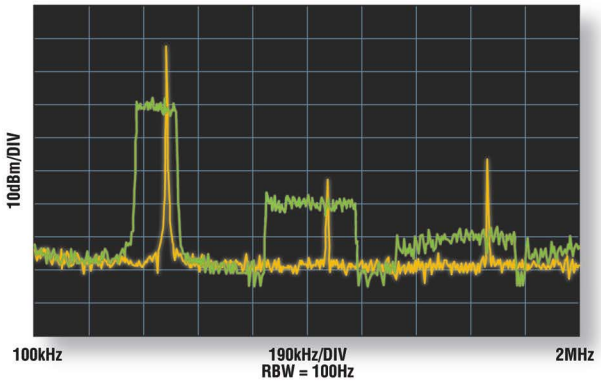


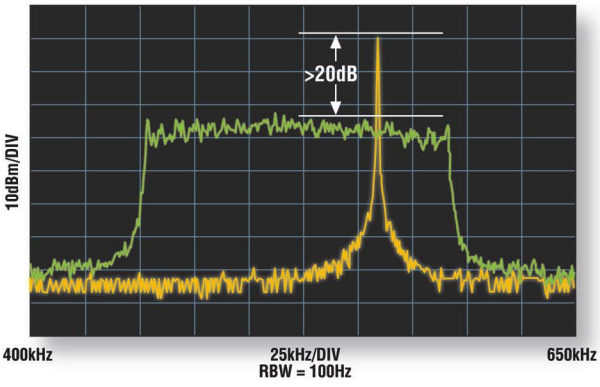

Figure 7 When the interconnection between the driver and the receiver is ac-coupled, the transitions at the receiver's input pins are detected by comparing the input signal with a delayed version of itself.

# Cut Switcher EMI >20dB

### Fundamental and Harmonic Frequencies




### Fundamental Frequency




Spread Spectrum Enabled

Spread Spectrum Disabled

## Eliminate Noise Problems with On-Chip Spread Spectrum

Built-in spread spectrum modulation in Linear Technology's new family of DC/DC regulators reduces peak radiated and conducted energy at any frequency by at least 20dB. This improvement significantly suppresses peak electromagnetic interference (EMI), reducing the need for metallic shielding or expensive filtering. Many of our future switching regulators will incorporate this technology – see the table below for our current offering.

## DC/DC Converters with Spread Spectrum Modulation

| Part Number | Step-Down Switching Regulators | $V_{IN}$ (V) | $V_{OUT}$ (V) | $I_{OUT}$ (A) | Tracking | PLL | Fixed Frequency (kHz) | Spread Spectrum Frequency Range (When Enabled) (kHz) | Package |
|---|---|---|---|---|---|---|---|---|---|
| **LTC®3736-1** | 2-Phase, Dual Synchronous Controller | 2.75 to 9.8 | 1: 0.6 to $V_{IN}$<br>2: 0.6 to $V_{IN}$ | 5 | ✓ | - | 300, 550 or 750 | 450 to 580 | QFN-24<br>SSOP-24 |
| **LTC3808** | Synchronous Controller | 2.75 to 9.8 | 0.6 to $V_{IN}$ | 5 | ✓ | ✓ | 300, 550 or 750 | 460 to 635 | DFN-14<br>SSOP-16 |
| **LTC3776** | DDR Memory Dual Controller | 2.75 to 9.8 | 1: 0.6 to $V_{IN}$<br>2: $V_{DDQ}$/2 | 5 | ✓ | ✓ | 300, 550 or 750 | 450 to 580 | QFN-24<br>SSOP-24 |
| **LTC3809** | Synchronous Controller | 2.75 to 9.8 | 0.6 to $V_{IN}$ | 5 | - | ✓ | 300, 550 or 750 | 450 to 580 | DFN-10<br>MSOP-10 |
| **LTC3252** | Inductorless, Dual, 2-Phase | 2.7 to 5.5 | 1: 0.9 to 1.6<br>2: 0.9 to 1.6 | 0.25 | - | - | - | 1,000 to 1,600 | DFN-12 |
| **LTC3251** | Inductorless, 2-Phase | 2.7 to 5.5 | 0.9 to 1.6 | 0.5 | - | - | 1,600 | 1,000 to 1,600 | MSOP-10 |
| **LTC3445** | Monolithic, $I^2C$, Triple Output | 2.5 to 5.5 | 1: 0.85 to 1.55<br>2, 3: ≥ 0.3 | 1: 0.6<br>2,3: 0.05 | ✓ | - | 1,500 | Adjustable Spread 0% to 22.4% | QFN-24 |
| **LTC3415** | Monolithic, PolyPhase, Stackable | 2.5 to 5.5 | 0.6 to $V_{IN}$ | 7 x n | ✓ | ✓ | 2,000 | 1,000 to 3,000 | QFN-38 |

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figuration) of programmable devices. In the past, suppliers of programmable ICs have used programming algorithms that differed not only among vendors, but also among device families from the same vendor.

The silicon portion of IEEE 1532 establishes common device behavior during programming via the IEEE 1149.1 state machine. The software portion of the standard defines a modified BSDL (boundary-scan-description-language) file, which extends to cover the new ISC instructions. Additionally, a new ISC data-file format contains all of the device and pattern-specific programming information.

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By delivering faster programming and facilitating more efficient use of expensive testers, the ISC features of 1532-compliant ICs provide significant savings to equipment manufacturers. Users will now be able to program chains of complex PLDs from multiple vendors using the same third-party programming tools and controllers.

Users will no longer need vendor-specific programming knowledge and will be able to concurrently program multiple PLDs from different IC vendors. Devices that are programmed concurrently instead of sequentially will simultaneously enter and leave programming wait states, minimizing configuration time, significantly reducing overall programming time, and allowing design needs, rather than programming-equipment availability, to govern programmable-device selection. **EDN**

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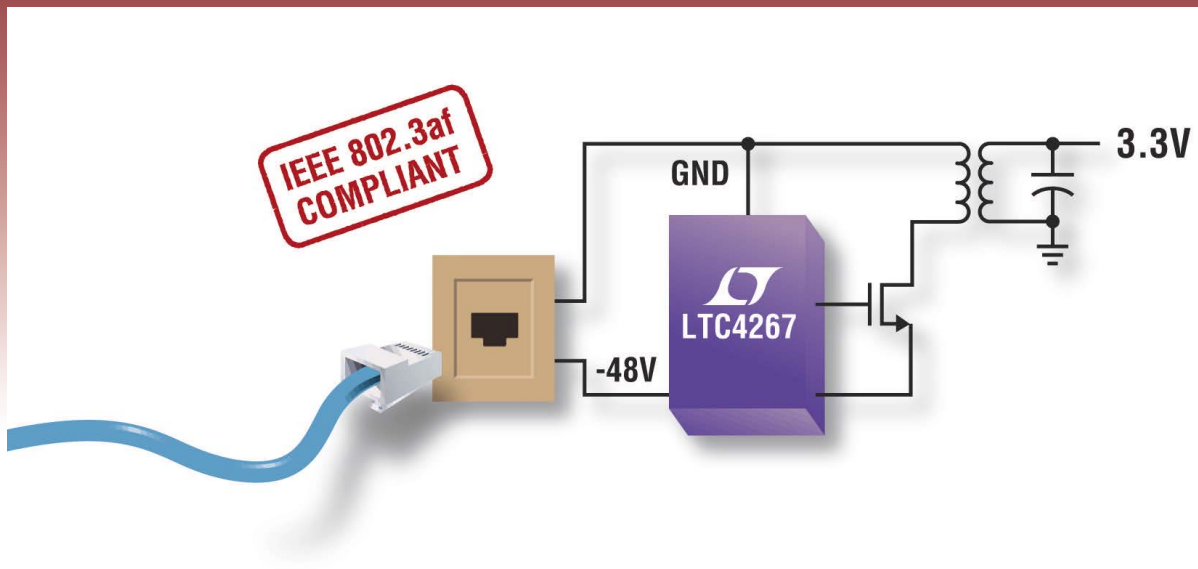
## AUTHOR'S BIOGRAPHY


*Peter Collins has worked in the test industry for 25 years and now works for JTAG Technologies in technical marketing. Before joining JTAG, he worked for eight years with Motorola in Swindon, UK, where he developed test approaches for GSM base-station pc boards. He was also jointly responsible for defining Motorola's corporate strategy for implementing 1149.1 in the factory and in the field. You can reach him at petec@jtag.co.uk.*

# Simple PoE Power

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- Onboard 25kΩ Signature Resistor
- Programmable Classification Current (Class 0-4)
- Integrated Error Amplifier and Voltage Reference
- 16-Pin SSOP and 3mm x 5mm DFN Packages
- LTC4267: $2.10 each in 1k Qty.

| Part Number | PD/PSE | Features |
|---|---|---|
| LTC4267 | PD | Integrated DC/DC Converter |
| LTC4257 | PD | Rugged, IEEE 802.3af Compliant |
| LTC4257-1 | PD | Rugged, Legacy Support |
| LTC4259A | PSE | Quad, IEEE 802.3af Compliant, AC-Disconnect |
| LTC4258 | PSE | Quad, IEEE 802.3af Compliant |

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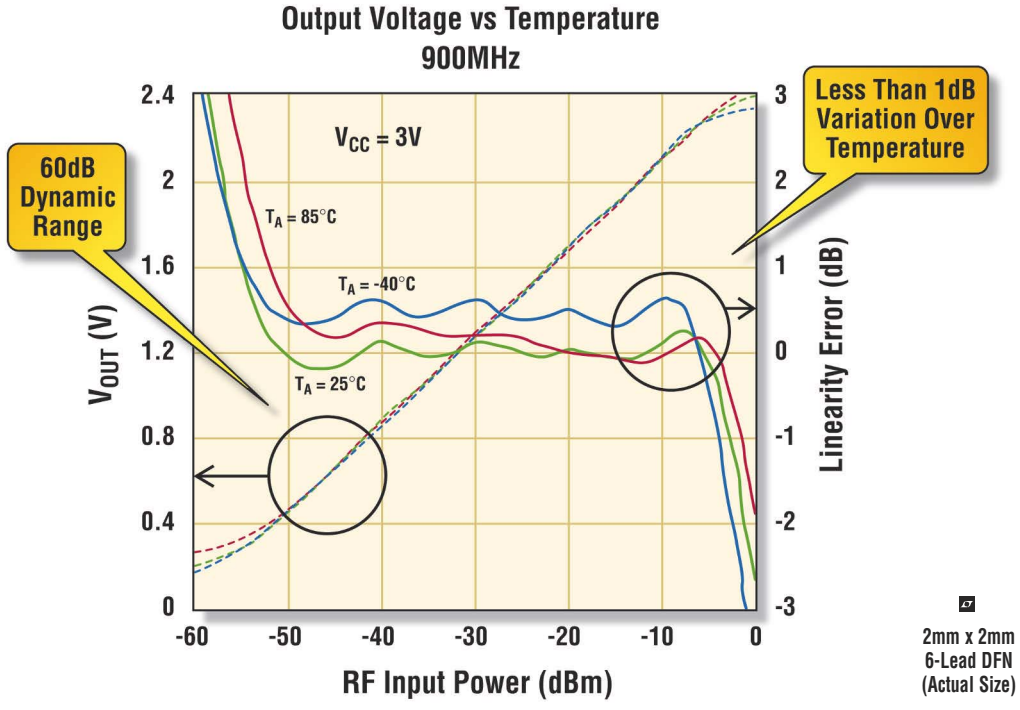


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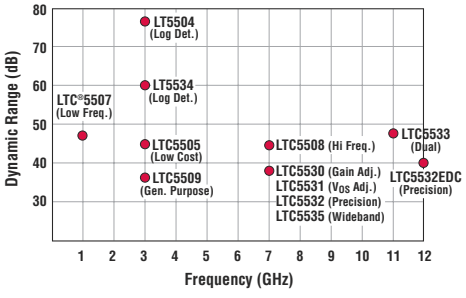


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# designideas

READERS SOLVE DESIGN PROBLEMS

## Buffer amplifier and LED improve PWM power controller's low-load operation

Gregory Mirsky, LaMarche Manufacturing Co, Des Plaines, IL

Texas Instruments' UCC3895 offers a good base for building a high-efficiency, pulse-width-modulated, switched-mode power supply that suits either current- or voltage-mode control. Designed for driving a full-bridge power inverter using two sets of complementary outputs, Out A through D, the circuit controls power by phase-shifting outputs C and D with respect to A and B. The manufacturer's data sheet provides a detailed description (**Reference 1**). However, when lightly loaded and configured for current-mode control, the controller can produce asymmetric-width pulses on its lagging outputs, C and D, under start-up conditions. **Reference 2** provides a complete description of the problem and a workaround.

Unfortunately, the workaround evokes other problems when you use the IC in other circuit implementations. **Figure 1**, from **Reference 2**, shows a partial schematic featuring the UCC3895 in a peak-current-mode-control circuit in which $R_1$ serves as a pullup resistor, providing a dc offset for the voltage ramp. However, for a significant portion of the ramp waveform, diode $D_1$ doesn't conduct and therefore narrows the power supply's dynamic range by cutting off a portion of the ramp voltage at $IC_1$'s Pin 3.

**Figure 2** shows another approach that requires additional components but delivers the full magnitude of the voltage ramp to Pin 3 of $IC_1$ and provides the approximately 1V-dc offset that **Reference 1** requires. Transistors $Q_1$ and $Q_2$, resistors $R_1$ and $R_2$, and LED $D_3$ form an emitter-follower amplifier for the ramp voltage available at $IC_1$, Pin 7 across timing capacitor $C_1$. This arrangement provides reliable current-mode operation over the full range from no-load to full-load output current by delivering a

### DIs Inside



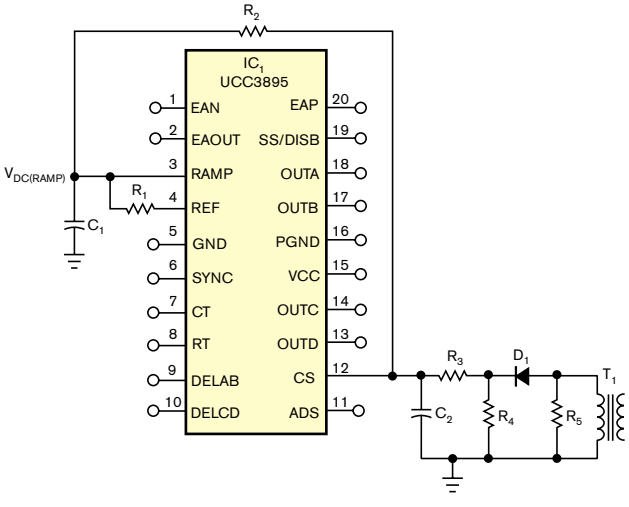


Figure 1 An added resistor, $R_1$, helps improve light-load operation of a popular switched-mode power-supply controller by eliminating output asymmetry.

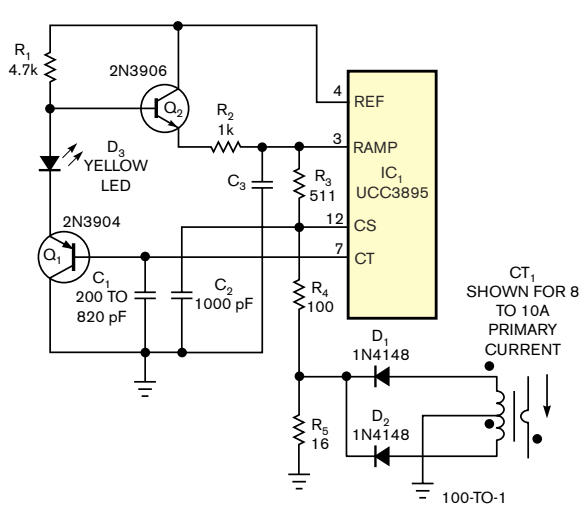


Figure 2 For even better performance, add a level-shifting amplifier to the ramp-voltage path.

sawtooth drive with a dc offset to $IC_1$'s ramp input. Diode $D_3$, a yellow LED, performs a 1.7V level translation without introducing any substantial signal loss. The component values not shown depend on the application. EDN


**REFERENCES**

1 "UCC3895 BICMOS Advanced Phase Shift PWM Controller," Texas Instruments data sheet, http://focus.ti.com/docs/prod/folders/print/ucc3895.html.

2 Mappus, S, "UCC3895 OUTC/OUTD Asymmetric Duty Cycle Operation," Texas Instruments Application Report, SLUA275, September 2002.


# Temperature controller has "take-back-half" convergence algorithm

W Stephen Woodward, University of North Carolina, Chapel Hill, NC

"The unfortunate relationship between servo systems and oscillators is very apparent in thermal-control systems," says Linear Technology's Jim Williams (**Reference 1**). Although high-performance temperature control looks simple in theory, it proves to be anything but simple in practice. Over the years, designers have devised a long laundry list of feedback techniques and control strategies to tame the dynamic-stability gremlins that inhabit temperature-control servo loops. Many of these designs integrate the temperature-control error term $T_S-T$ in an attempt to force the control-loop error to converge toward zero (**Reference 2**).

One tempting and "simple" alternative approach makes the heater power proportional to the integrated temperature error alone. This "straight-integration" algorithm samples the temperature, T, and subtracts it from the setpoint, $T_S$. Then, on each cycle through the loop, the loop gain, F, multiplies the difference, $T_S-T$, and adds it as a cumulative adjustment to the heater-power setting, H. Consequently, $H=H+F\times(T_S-T)$.

The resulting servo loop offers many desirable properties that include simplicity and zero steady-state error. Unfortunately, as **Figure 1** shows, it also exhibits an undesirable property: an oscillation that never allows final convergence to $T_S$. Persistent oscillation is all but inevitable because, by the time that the system's temperature corrects from a deviation and struggles back to $T=T_S$, the heater power inevitably gets grossly overcorrected. In fact, the resulting overshoot of H is likely to grow as large as the original perturbation. Later in the cycle, H's opposite undershoot grows as large as the initial overshoot, and so on.

Acting on intuition, you might attempt to fix the problem by adopting a better estimate of H whenever the system's temperature crosses the setpoint, $T=T_S$). This Design Idea outlines a TBH (take-back-half) method that takes deliberate advantage of the approximate equality of straight-integration's undamped overshoots and undershoots. To do so, you introduce variable $H_O$ and run the modified servo loop, except for the instant when the sampled temperature, T, passes through the setpoint, $T=T_S$. Whenever a setpoint crossing occurs, the bisecting value $(H+H_O)/2$ replaces both H and $H_O$. As a result, at each setpoint crossing, H and $H_O$ are midway between the values corresponding to

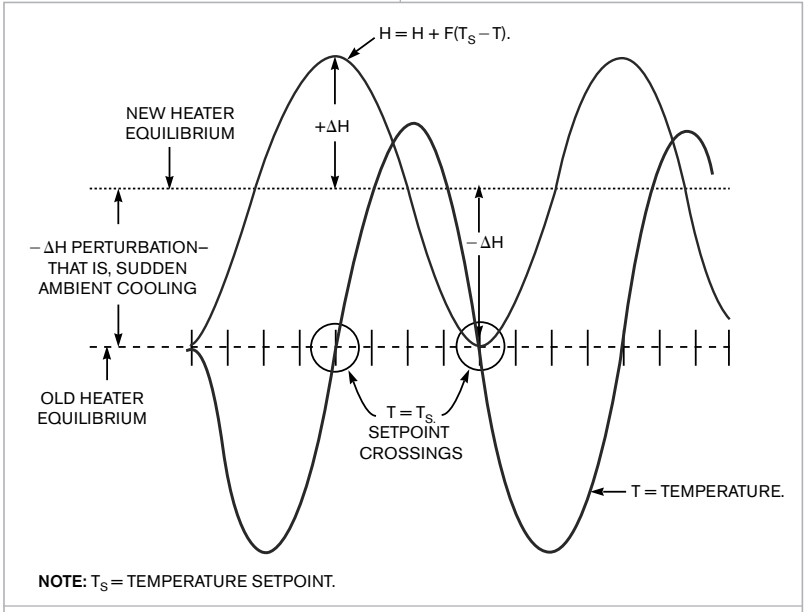


Figure 1 A simple integrating control algorithm virtually guarantees that the system's temperature oscillates and never converges to the setpoint temperature, $T_S$.

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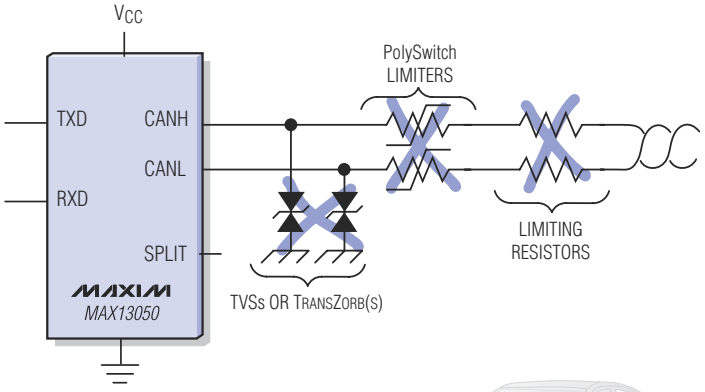


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| ESD Protection IEC Contact Discharge** (kV) | ±8 | — | ±8 | — | ±8 | — | ±8 | — |
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the current (H) and previous ($H_O$) crossings. This action takes back half of the adjustment applied to the heater setting between crossings. **Figure 2** shows how a simulated TBH algorithm forces rapid half-cycle convergence.

Successful applications of the TBH algorithm range from precision temperature control of miniaturized scientific instrumentation to managing HVAC (heating/ventilation/air-conditioning) settings for crew rest areas in Boeing's 777 airliner. Experience with TBH applications shows that, with a reasonable choice for loop gain, F, the algorithm exhibits robust stability.

In general, a TBH system's natural cycle time is proportional to the square root of the ratio of the thermal time constant to F. Based on both simulations and experiments, a cycle time that's at least eight times longer than

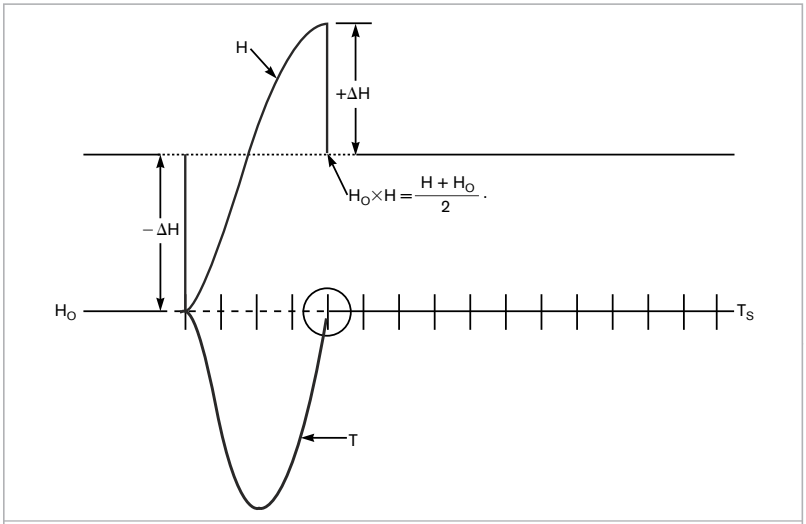
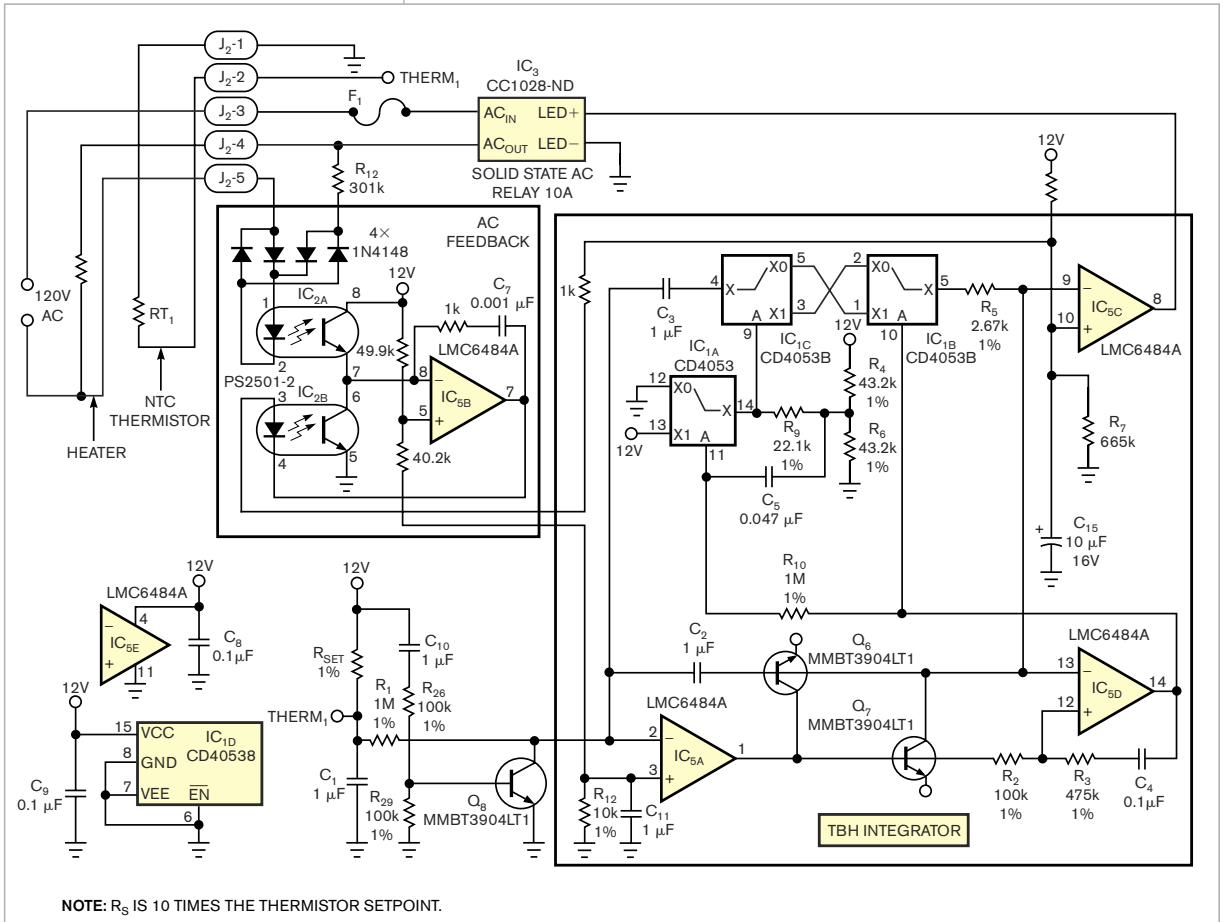



Figure 2 In this simulation, applying the "take-back-half" algorithm forces convergence to the setpoint value in a single half-cycle.




**NOTE:** $R_S$ IS 10 TIMES THE THERMISTOR SETPOINT.

Figure 3 For safety, this version of a TBH heater controller features full isolation of the ac-line and control circuits.

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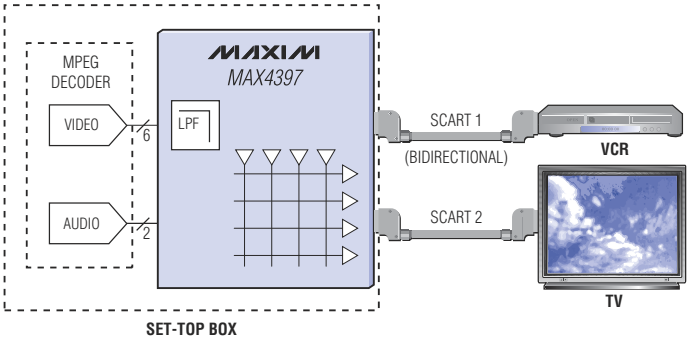


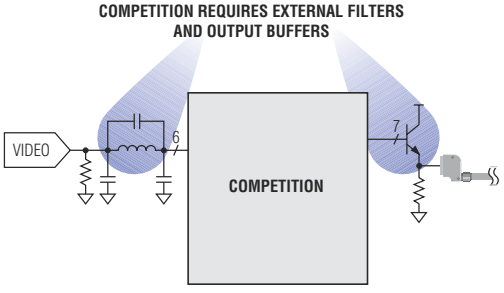


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| MAX4397S | 2 | Yes | Yes | Single-ended | Yes | Programmable | 5 and 12 |
| MAX4399 | 3 | No | Yes | Single-ended | Yes | Programmable | 5 and 12 |

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the heater-sensor time delay ensures convergence. Therefore, setting loop gain F low always achieves convergence, and the steady-state error, $T_S-T$, remains equal to zero.

**Figure 3** shows a practical example of a TBH controller that's suitable for managing large thermal loads. Thermistor $RT_1$ senses heater temperature. The output of error-signal integrator $IC_{5A}$ ramps negative when $T<T_S$ and ramps positive when $T_S>T$, producing a control signal that's applied to comparator $IC_{5C}$, which in turn drives a solid-state relay, $IC_3$, which is rated for 10A loads.

Comparator $IC_{5D}$ and the reverse-parallel diodes formed by the collector-base junctions of $Q_6$ and $Q_7$, and the CMOS switches of $IC_1$ perform the TBH zero-crossing convergence function.

In most temperature-control circuits, it's advantageous to apply a reasonably linear feedforward term that represents the actual ac voltage applied to the heater; the need for complete galvanic isolation between the control and the power-handling circuits complicates this requirement. In this example, a linear isolation circuit comprising a PS2501-2 dual-LED/phototransistor optoisolator ($IC_{2A}$ and $IC_{2B}$) and op-amp $IC_{5B}$ delivers feedback current to $C_{15}$ and $IC_{5C}$ that's proportional to the averaged ac heater current. As a bonus, the feedback circuit provides partial instantaneous compensation for ac-line voltage fluctuations. EDN

## REFERENCES


1 Williams, Jim, *Linear Applications Handbook*, Linear Technology, 1990.
2 "Hybrid Digital-Analog Proportional-Integral Temperature Controller," www.discovercircuits.com/C/control3.htm.


# MOSFET enhances low-current measurements using moving-coil meter

Stefan Strózecki, Institute of Telecommunications ATR, Kaliskiego, Poland

A previous Design Idea describes an interesting and useful method for using a moving-coil analog meter to measure currents in the less-than-1A range (**Reference 1**). The design offers considerable flexibility in the choice of meter-movement sensitivity and measurement range and simplifies selection of shunt resistors. Although the design uses a bipolar meter-driver transistor, under some circumstances, a MOSFET transistor represents a better choice. The original circuit comprises a voltage-controller current sink that measures the bipolar transistor's emitter current, but the transistor's collector current drives the analog meter. A bipolar transistor's emitter and collector currents, $I_E$ and $I_C$, respectively, are not identical because base current, $I_R$, adds to the emitter current.

You can express these current components as $I_E=I_C+I_B$ and then as $I_C=I_E-I_B$. Whether base current adversely affects the measurement accuracy depends on the magnitude of $I_B$ and the magnitude of the common-emitter current gain, $\beta$, because base current $I_B=I_C/\beta$. When $\beta$ is greater than 100, the base current's contribution to emitter current is generally negligible. However, $\beta$ is sometimes smaller. For example, the general-purpose BC182, an NPN silicon transistor, has a low-current $\beta$ of only 40 at room temperature. If you were to use a 15-mA-full-scale meter in the transistor's collector, full-scale base current $I_B$ at minimum $\beta$ would amount to 0.375 mA. Subtracting base current from collector current introduces a 2.5% error.

But if you use a moving-coil meter that requires 150 µA for full-scale deflection, the measurement error increases considerably because $\beta$ decreases as collector current decreases. For the BC182, reducing collector current from a few milliamps to 200 µA, current gain decreases $\beta$ by a factor of 0.6 and adversely affects the meter reading's accuracy.

To solve the problem and improve the circuit's accuracy, you can replace the

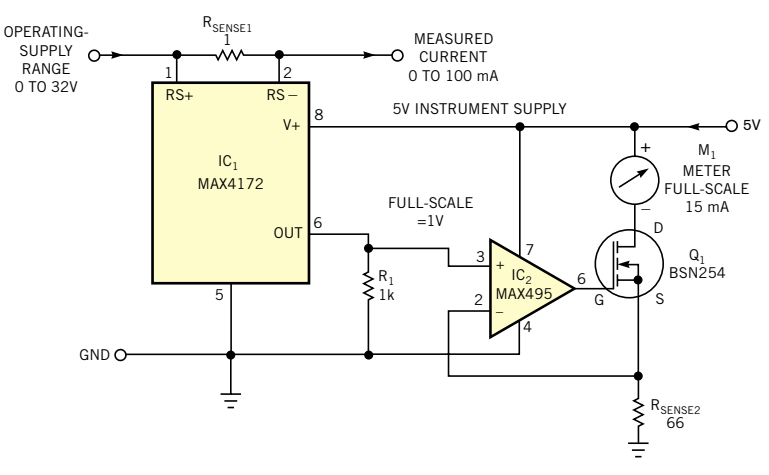


Figure 1 This updated version of an earlier Design Idea uses a MOSFET to drive an analog meter display, offering great flexibility in power-supply-current measurement.

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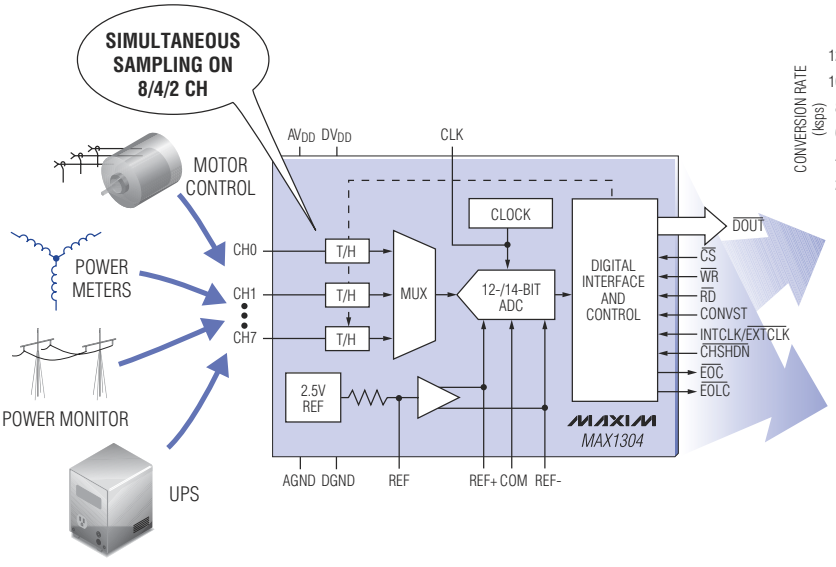


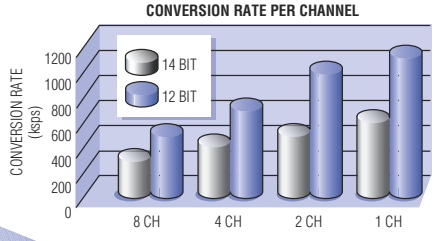


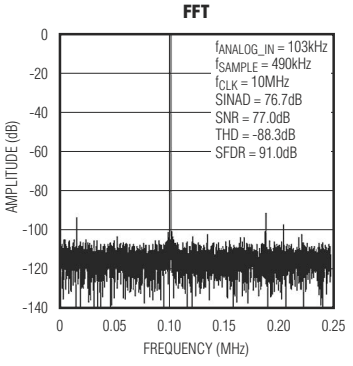


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| MAX1308–MAX1311 | 12 | 8/4/2/1 | ±5 | 71 | -83 | 71 | 10.49/7.95/6.97/6.49 |
| MAX1312–MAX1315 | 12 | 8/4/2/1 | ±10 | 71 | -83 | 71 | 10.49/7.95/6.97/6.49 |
| MAX1316–MAX1319 | 14 | 8/4/2/1 | 0 to 5 | 77 | -90 | 76.5 | 15.75/11.25/10.75 |
| MAX1320–MAX1323 | 14 | 8/4/2/1 | ±5 | 77 | -90 | 76.5 | 20.25/13.50/11.97 |
| MAX1324–MAX1327 | 14 | 8/4/2/1 | ±10 | 77 | -90 | 76.5 | 20.25/13.50/11.97/10.96 |

†1000-up recommended resale. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

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BC182 with an N-channel MOSFET, such as the BSN254 (**Figure 1**). Because a MOSFET draws no gate current, its drain current, $I_D$, equals its source current, $I_S$. When you select a MOSFET for the circuit, note that the device's gate-source threshold voltage should be as low as possible. For example, the BSN254 has a room-temperature gate-source threshold-voltage range of 0.8 to 2V. The remainder of the circuit design proceeds as in the original Design Idea; that is, for a maximum voltage drop of 1V across $R_1$, you calculate $R_{SENSE2}$ as follows: $R_{SENSE2}=(1V/I_{METER})$, where $R_{SENSE}$ is in ohms, 1V represents the voltage drop across $R_1$, and $I_{METER}$ is the full-scale meter reading in amps. Note that a 1-kΩ resistor at $R_1$ develops 10V/1A output across sense resistor $R_{SENSE1}$. In this application, 100 mA produces 0.1V across $R_{SENSE1}$, and the voltage across $R_1$ thus corresponds to 1V for full-scale deflection of the meter. EDN

## REFERENCE

1 Bilke, Kevin, "Moving-coil meter measures low-level currents," *EDN*, March 3, 2005, pg 72, www.edn.com/article/CA505070.

# Shunt regulator serves as inexpensive op amp in power supplies

Michael O'Loughlin, Texas Instruments, Nashua, NH

Developed as a three-terminal shunt regulator, the popular and multiple-sourced TL431 IC offers designers many intriguing possibilities beyond its intended application. Internally, the TL431 comprises a precision voltage reference, an operational amplifier, and a shunt transistor (**Figure 1a**). In a typical voltage-regulator application, adding two external resistors, $R_A$ and $R_B$, sets the shunt-regulated output voltage at the lower end of load resistor $R_S$ (**Figure 1b**).

In today's power-supply market, cost reduction drives most designs, as evidenced by Asian manufacturers that have resorted to shaving pennies off their power-supply products by using single-sided pc boards. This Design Idea shows how a three-terminal shunt regulator can replace a more expensive conventional operational amplifier in a power-converter design.

A switched-mode power supply uses a galvanically isolated feedback portion of a PWM circuit (**Figure 2**). In designs that omit a voltage amplifier, a shunt regulator can serve as an inexpensive op amp. Resistors $R_1$ and R set the power supply's dc output voltage, and optocoupler $IC_2$ provides galvanic isolation. Resistor $R_1$ provides bias for the optocoupler and the TL431, $IC_1$. Resistor $R_3$ and zener diode $D_1$ establish a fixed bias voltage to ensure that bias resistor $R_1$ does not form a feedback path. Resistors $R_1$ and $R_2$ control the gain across the optocoupler. In most designs, the ratio of $R_2$ to $R_1$ is roughly 10-to-1.

Components $C_P$, $C_Z$, and $R_Z$ provide frequency compensation for the control loop. The optocoupler includes a high-frequency pole, $f_P$, in its frequency response, an item that most optocouplers' data sheets omit. You can use a network analyzer to determine the location of the high-frequency pole or estimate that the pole occurs at approximately 10 kHz. The following **equation** describes the compensation network's small-signal transfer function:

$$G_C(s)=\frac{\Delta V_{ERR}}{\Delta V_{OUT}}=\frac{(s\times R_Z\times C_Z+1)}{s\times R_1(C_Z+C_P)\left(\frac{s\times R_Z\times C_P\times C_Z}{C_P+C_Z}+1\right)}\times\frac{R_2}{R_1}\times\left(\frac{1}{\left(\frac{s}{2\times\pi\times f_P}+1\right)}\right).$$

Note that, under some circumstances, adding a bypass capacitor across diode $D_1$ may be necessary for output-noise reduction. EDN

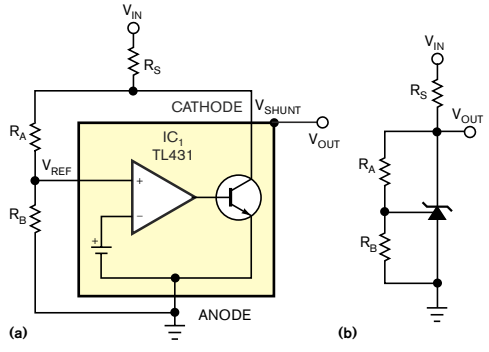


Figure 1 Despite the block diagram, the TL431 is internally complex (a), but you need only three external resistors to use the TL431 in a basic shunt-regulator circuit (b).

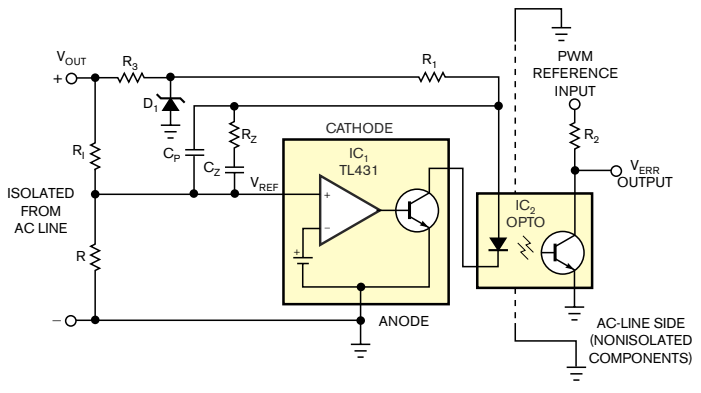


Figure 2 A TL431 replaces a more expensive operational amplifier in this power supply's PWM feedback-regulator circuit.

LINEAR TECHNOLOGY

DESIGN NOTES

# High Efficiency 2-Phase Boost Converter Minimizes Input and Output Current Ripple – Design Note 371

Goran Perica

## Introduction

Many automotive and industrial applications require higher voltages than is available on the input power supply rail. A simple DC/DC boost converter suffices when the power levels are in the 10W to 50W range, but if higher power levels are required, the limitations of a straightforward boost converter become quickly apparent. Boost converters convert a low input voltage to a higher output voltage by processing the input current with a boost inductor, power switch, output diode and output capacitor. As the output power level increases, the currents in these components increase as well. Switching currents also increase proportional to the output-to-input voltage conversion ratio, so if the input voltage is low, the switching currents can overwhelm a simple boost converter and generate unacceptable EMI.

For example, consider Figure 1, a 12V input to 24V, 10A output switching converter operating at 300kHz. The currents processed by the converter in Figure 1 are shown in the first row of Table 1. The relatively high current levels in the switcher are reflected in high input and output ripple currents, which results in increased EMI.



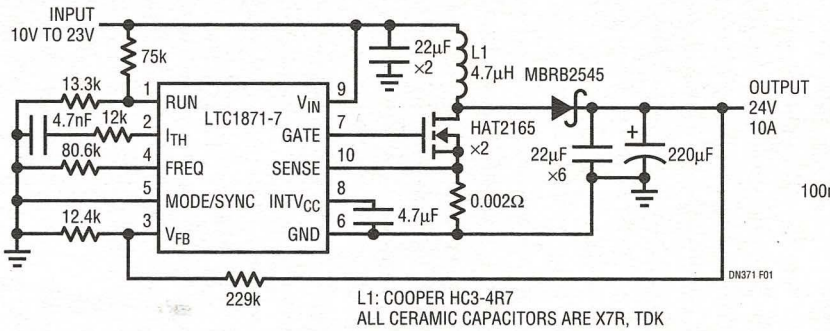


**Figure 1a. Single-Phase Boost Converter: Can be Used to Convert 12V Input to 24V, 10A Output**

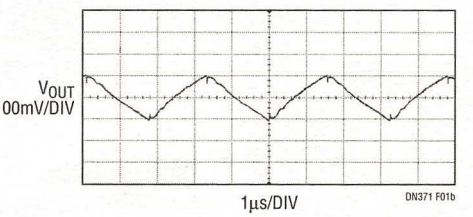


**Figure 1b. Single-Phase Boost Converter Output Voltage Ripple**

**Table 1. Dual-Phase Boost Converter Has Lower Input and Output Ripple Currents and Voltages Than Single-Phase Boost Converter**

| | INPUT RMS CURRENT | INPUT RIPPLE CURRENT | MOSFET RMS DRAIN CURRENT | OUTPUT DIODE RMS CURRENT | OUTPUT CAPACITOR RMS CURRENT | OUTPUT CAPACITOR FREQUENCY | OUTPUT VOLTAGE RIPPLE |
|---|---|---|---|---|---|---|---|
| **SINGLE-PHASE BOOST CONVERTER** | 21.1A | $4.2A_{P-P}$ | 15.4A | 14.4A | 10.5A | 300kHz | 212mV |
| **DUAL-PHASE BOOST CONVERTER** | 20.7A | **$0.17A_{P-P}$** | 2 × 7.4A | 2 × 7.2A | **1.9A** | 600kHz | **65mV** |

The circuit shown in Figure 2 performs the same DC/DC conversion, but with greatly reduced input and output ripple, significantly reducing EMI, and at a higher effective switching frequency, which allows the use of two 22µF output capacitors versus six 22µF output capacitors required in Figure 1.

The trick is the 2-phase boost topology, which interleaves two 180° out-of-phase output channels to mutually cancel out input and output ripple current—the results are shown in the second row of Table 1. Each phase operates at 50% duty cycle and the rectified output currents from each phase flow directly to the load—namely the low inductor ripple current—so only a small amount of output current (shown in Table 1) is handled by the output capacitors.

The centerpiece of the design in Figure 2 is the LT®3782 2-phase current mode PWM controller. Current mode operation ensures balanced current sharing between the two power converters resulting in even power dissipation between the power stages.

The efficiency of the dual-phase converter, shown in Figure 3, is high enough that it can be built entirely with surface mount components—no need for heat sinks. In a 240W boost supply application, the power dissipation of 12.9W is relatively easy to manage in a well laid out, large multilayer PCB with some forced airflow.

## Conclusion

The simple LT3782 dual-phase switching boost converter improves on single-phase alternatives by allowing high power output with lower ripple currents, reduced heat dissipation and a more compact design.

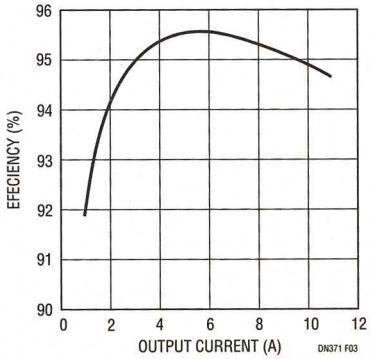


**Figure 3. 12V Input to 24V Output Dual-Phase Boost Converter Efficiency**

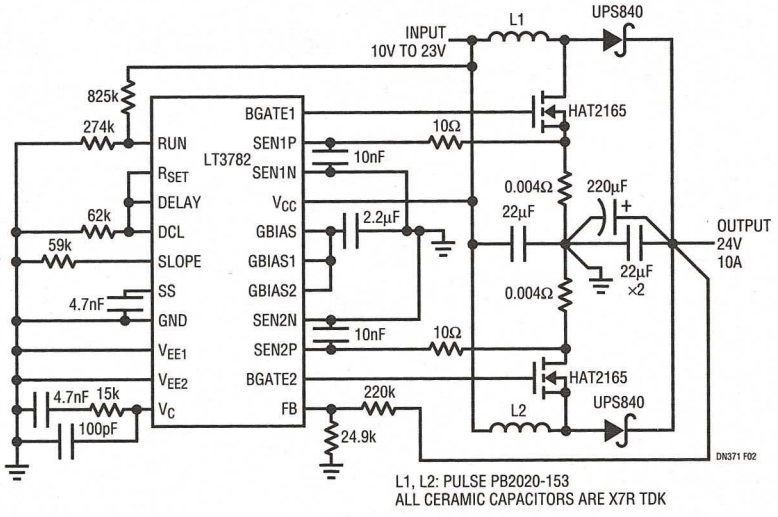


**Figure 2a. Dual-Phase Boost Converter Reduces EMI and Ripple Currents with a Minimum Input and Output Filtering**

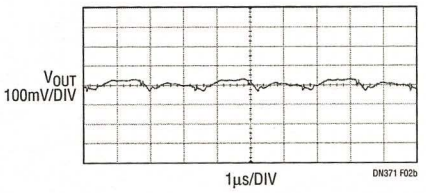


**Figure 2b. Dual-Phase Boost Converter Output Voltage Ripple**

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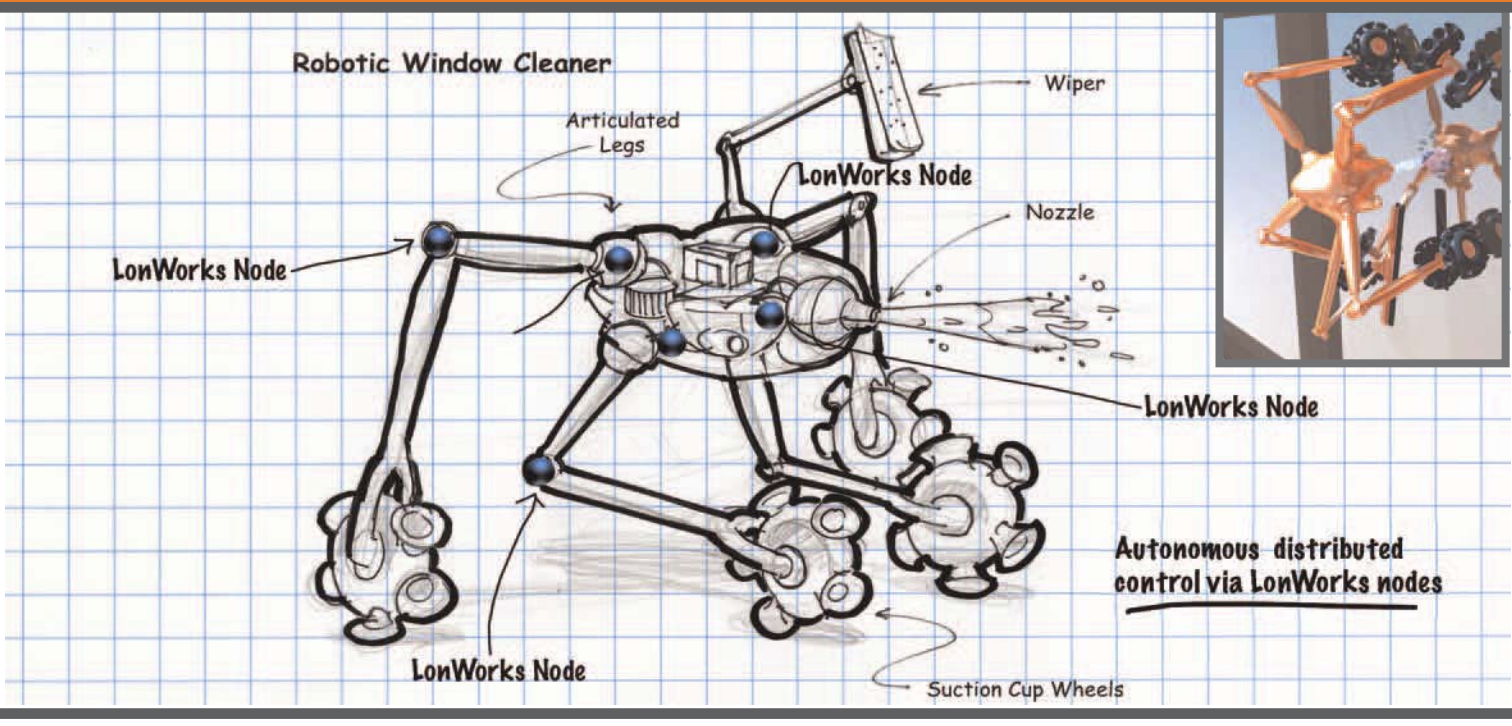


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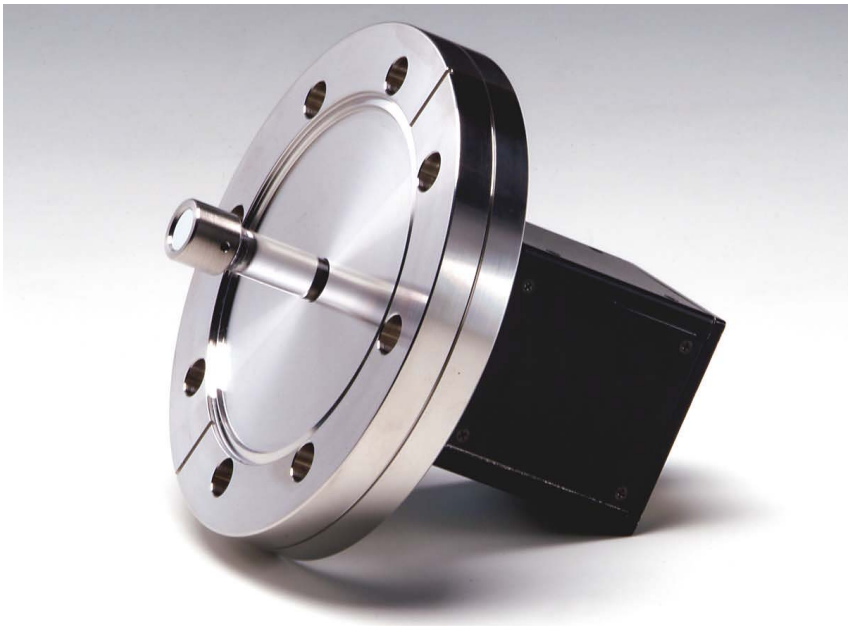
# productroundup

## SENSORS & TRANSDUCERS



### Unit features high-speed electron detection

The H8770 electron-detection unit incorporates a fast-decay phosphor and highly sensitive compact PMT (photomultiplier tube). For design into semiconductor-inspection systems and scanning electron microscopes, the unit has a phosphor decay time of 2.3 nsec, a gain range of $1\times10^2$ to $1\times10^6$, a typical noise level of 20 mV, and a detectable input-electron energy range of 5 to 12 keV. Features include a built-in PMT power supply, a high-voltage power supply, a voltage-divider circuit, and a high-speed amplifier with a bandwidth of 150 MHz. The H8770 electron-detection unit costs $8768 (small quantities).

**Hamamatsu Corp, www.hamamatsu.com**

### Noncontact rotary-position sensor enables custom output curve

Providing 360° absolute-angle measurements, the noncontacting RSC3700 rotary-sensor family features 12-bit resolution. Incorporating a microprocessor enables designers to preprogram a custom output-characteristic curve into the sensor for specific applications. Product specifications include ±0.09° resolution, ±0.1% linearity, less than 0.15% repeatability, and a 1-kHz sample rate. The output interfaces include ranges of 4 to 20 mA, 0 to 10V, or 0.5 to 4.5V analog and a digital PWM. The sensor refers measurements to a mechanical index point, allowing retention of position for power failures.

**Novotechnik, www.novotechnik.com**

### Sensor series measures barometric pressure

The MS5534B series of piezoresistive pressure sensors includes an ADC-interface IC and six readable coefficients for highly accurate software calibration. The sensors communicate with a microcontroller through a three-wire interface. The sensor measures from 0 to 1100 mbar (0 to 110 kPa), has a temperature range of −40 to +125°C, and has a power-supply requirement of 2.2 to 3.6V. In a $9\times9$-$mm^2$ package, the MS5534B costs $15 (1000).

**Servoflo, www.servoflo.com**

### Programmable sensor-interface IC targets automotive applications

Targeting use in resistive-bridge sensors, including pressure transducers, strain gauges, and position sensors, the MLX90320 calibrates the sensor output by nulling the offset voltage and applying the appropriate signal gain to calibrate the output-voltage span between 0 and 5V. An on-chip EEPROM stores digital coefficients that determine digital-calibration parameters. For accurate calibration, both gain and offset have coarse and fine DACs.

**Melexis, www.melexis.com**

### Proximity sensor targets automatic plumbing fixtures

Able to detect the presence of objects from a distance of 0.04 to 24 in. by means of a reflective sensor, the OPB720 series optical-proximity sensor features a synchronized infrared LED and photosensor. It can switch from high level with no reflection target to low level with reflection. The series suits automatic plumbing fixtures, using a dc current of 50 mA with power dissipation of 300 mW. Measuring $1.1\times0.68\times0.33$ in., the OPB720 series costs $31.05 (1000).

**Optek Inc, www.optekinc.com**

# productroundup

## SENSORS & TRANSDUCERS

### Sensor ICs have low power consumption

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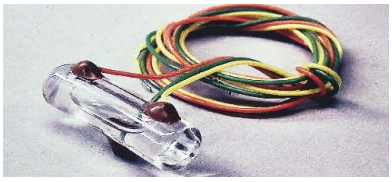
**ZMD America, www.zmda.com**

### Single-axis tilt sensor targets high-accuracy applications

The single-axis output electrolytic tilt sensor features a ±30-arc minimum-angle range, less than 0.05-arc/sec resolution, and less than 0.5-arc/sec null repeatability. Also referred to as a precision contact level, the device has a hermetic glass-to-metal



construction with platinum electrodes, suited for high-accuracy and linear-output applications.
**Fredericks Co, www.fredericks com.com**

## MICROPROCESSORS

### Reconfigurable processor adds DSP for wireless applications

The STW22000 multipurpose-microcontroller family now includes a 600-MHz, 16/32-bit dual-MAC (multiply-accumulate)-unit DSP core. The device comprises a 300-MHz ARM926EJ-S RISC core, 16 Mbytes of embedded DRAM, and an eFPGA (embedded field-programmable-gate-array) block. The microcontroller also features an embedded, dedicated convolutional decoder engine and a set of embedded DSP-core developmental tools for performance evaluation and on-chip application-code development, debugging, and integration in an ARM/DSP environment, allowing multicore-development and debugging. The STW22000 comes with a board-support package supporting multiple OS implementations, as well as additional software elements available through the ST122 DSP core.

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**STMicroelectronics, www.st.com**

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**Freescale Semiconductor, www.freescale.com**



## Microcontroller families are ROHS-compliant

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**Goal Semiconductor, www.goalsemi.com**

## 8-bit microcontroller has increased functions at low cost

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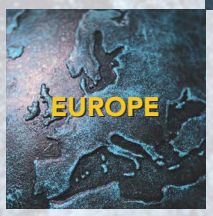


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STATS 3 million/week shipments by mid-2004 / 5 million/week by mid-2005 / SIG has 3400 members

## Bluetooth ramps slowly, then soars

Bluetooth's developers began work on the technology in 1995. They intended that Bluetooth become a replacement for short-distance, moderate-bandwidth links, such as between PCs and peripherals or music players and headsets. When the Bluetooth SIG (Special Interest Group) formed in 1998, major industry players Ericsson, IBM, Intel, Nokia, Toshiba, Microsoft, and Motorola joined the effort, culminating in the emergence in 1999 of Version 1.0A of the specification. Promoters and analysts expected fast adoption and quick, wide availability of end products. Although the first retail products did appear in 2001, their emergence was just a trickle, due to revisions in the specification; interoperability, security, and verification issues; challenges in developing the requisite ICs; complexity of the protocol and stack; and end-user unfamiliarity.

However, by the summer of 2004, shipments of Bluetooth chip sets reached 3 million per week, up from 2 million just a few months earlier, and, by mid-2005, they reached 5 million per week, corresponding to an estimated IC revenue of $1 billion for the year. Analysts say that most Bluetooth applications are for wireless headsets in mobile phones, other portable devices, and automotive applications. The Bluetooth SIG now has more than 3400 members; chip-set prices have dropped to approximately $5.—by Bill Schweber

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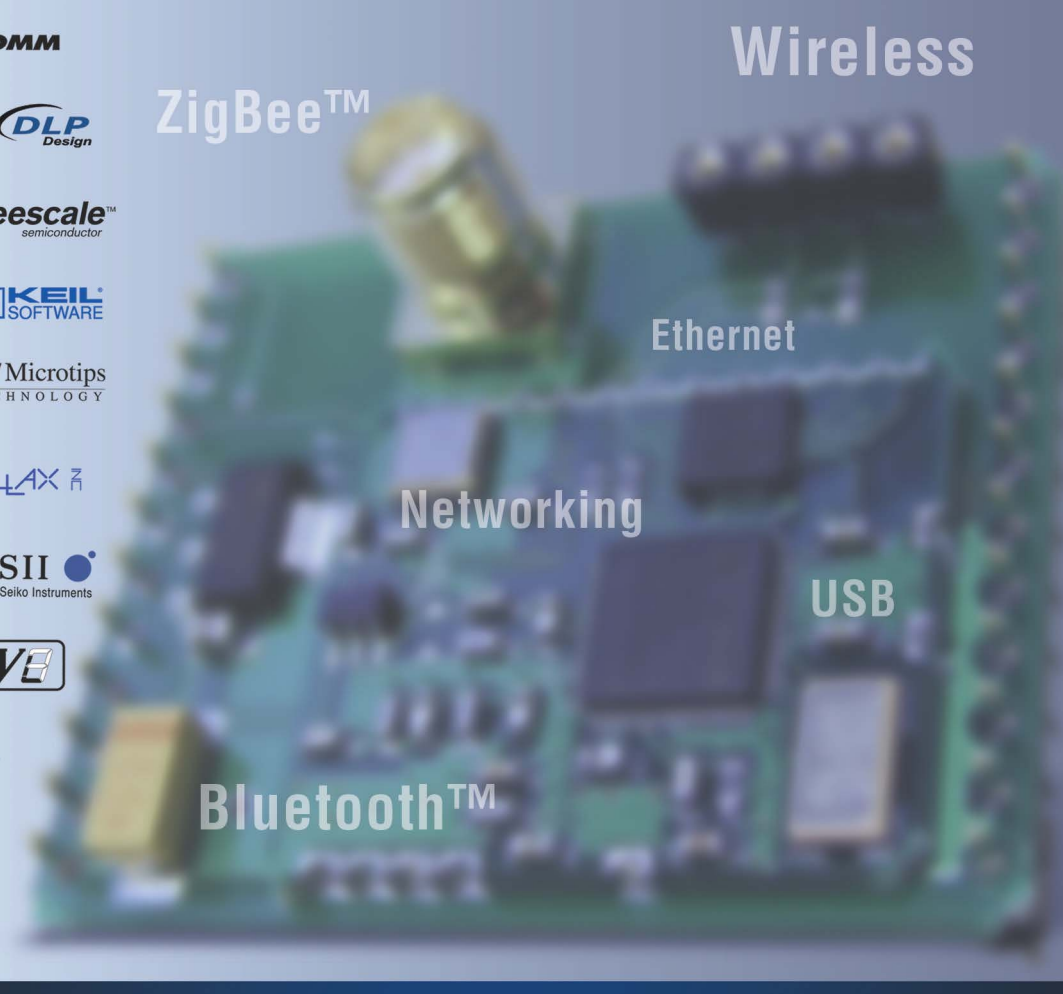


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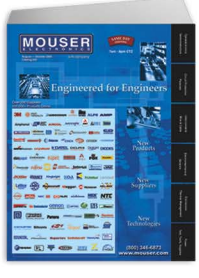


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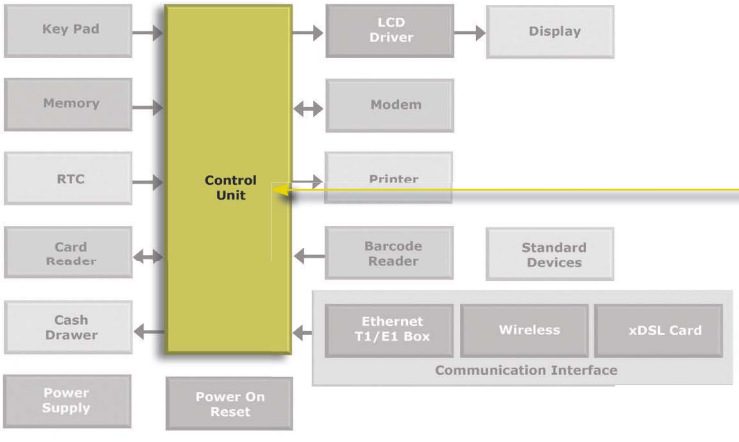


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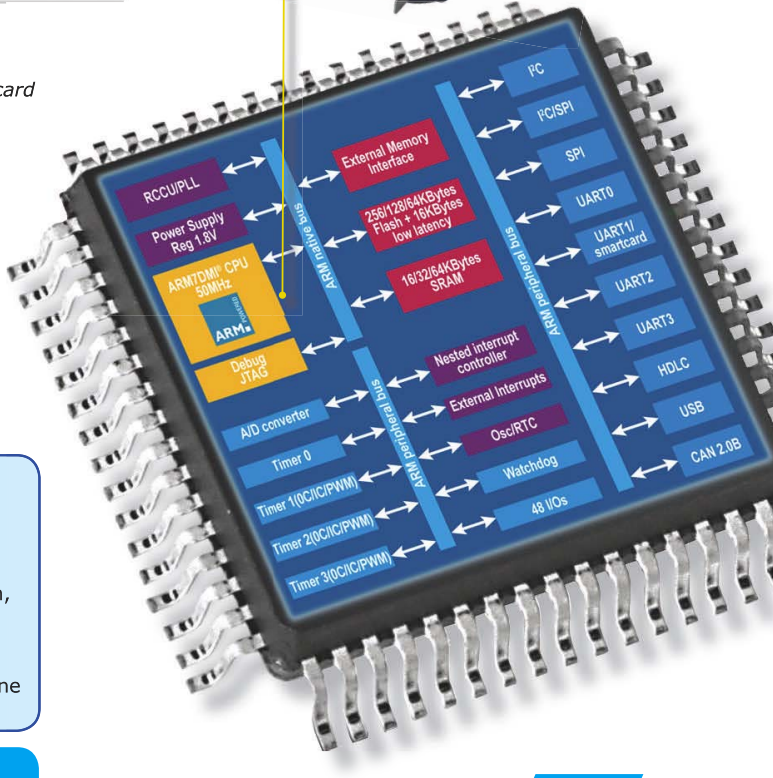


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